Hardware Project for CMPE310
Total 100 points. Extra Credit 50 points.
Assigned: Friday, April 19
Due (for extra credit): Friday, April 26 (midnight)
Due (without extra credit): Thursday, May 1 (midnight)

Project Description: Design a memory system in Concept-HDL for 80286/80386.
Design a memory system for the 80286/80386 processors. These processors have a 24-bit address bus and 16-bit data bus. The memory system should have separate high and low banks and should be able to read and write a byte or 16-bits. Use separate bank decoders for high bank and low banks. Do not use separate write and read signals for the banks. Also don't use Vcc and Gnd in the circuit and decode using only the address and BHE_. The system specifications are given below:

Parameter	Specification
Project Name and Directory Name	310_Proj5
Libraries to be included	a74ttl, a74lsttl, memory
Design Name	project5

The memory system will have one EPROM section and two SRAM sections as described below.

EPROM Section
The EPROM section contains 256K 16-bit memory and should use the 27512 64Kx8 EPROM. The address range for the EPROM section is F80000H-FFFFFFH. Access time for this EPROM is atleast 250ns. It takes a parameter called MEMORYFILE from which the EPROM locations are loaded.

SRAM Section I
This SRAM section contains 256K 16-bit memory and should use IDT71256 32Kx8 SRAMs. The address range for this section is F00000H-F7FFFFH. Access time for this SRAM is atleast 100ns. The size parameter should be set to 8.

SRAM Section II
This section contains 64K 16-bit memory and should use CY7C194 64Kx4 SRAMs. The address range for this section is E60000H-E7FFFFH. Access time for this SRAM is atleast 12ns. The size parameter should be set to 4.

For decoding you can use whatever chips you want. You will be graded on the number of chips that you use for decoding. Use minimum number of chips required to do the decoding. You will have to do a multi-page schematic as the project will have a lot of chips.

Verilog Models
If you are interested in looking at the verilog models for these devices you can go to: */cs/psd/share/library/ver_<library_name>* and then the *chip_name* you are using. There will be a *vlog_model* directory under which there will be a *verilog.v* file.

Extra Credit (Verilog Test Bench)

When you save the design it creates the verilog file for the design and saves it under *<project_directory>/worklib/<project_name>/sch_1/verilog.v*
You will generate the test bench for your design (using the one provided last time) for extra credit. Check the deadline and details for the submission. The test bench should load all the EPROMs with data using the MEMORYFILE parameter mentioned before. Then read the first and last location in each EPROM chip to make sure that the decoding is correct. Read 16-bits and single bytes to make sure that the bank architecture is correct. Then write 16-bit as well as a byte to each SRAM chip that you have. Read all these values back to make sure that you have written them properly. A test bench submitted without any of this requirements will get at the most only 50% of the extra credit. The name of the testbench file should be *project5_test.v.*

Input/Outputs

The following is the list of input/output ports of your design. Use the same name, size and direction as mentioned below. All the signals follow the intel architecture convention i.e. read, write and bhe are active low etc.You can use any other names for internal wires.

Signal Name	Direction	Size (bits)
address	IN	24
data	IO	16
read_	IN	1
write_	IN	1
bhe_	IN	1

Submission (both extra credit and regular)

Tar your project directory using *tar -cvf project5.tar <your_directory_name>*.
Gzip it using the command *gzip project5.tar.*
Submit the *project5.tar.gz* file.

Re-submission:
If you submit your project by the earlier deadline it will be considered for extra-credit. However, if you resubmit your project during the next regular deadline (i.e. after changing it) you will get at the most only 50% of extra credit. Make sure your project is correct during the first submission to avoid this. Don’t submit partly done or not-working projects in the earlier deadline. Your project will be considered for extra-credit only if it is fully functional at the time of the first submission.

ANY FORM OF CHEATING WILL RESULT IN A ZERO FOR THE PROJECT AND THE APPROPRIATE DISCIPLINARY ACTION AS MANDATED BY UNIVERSITY POLICY.