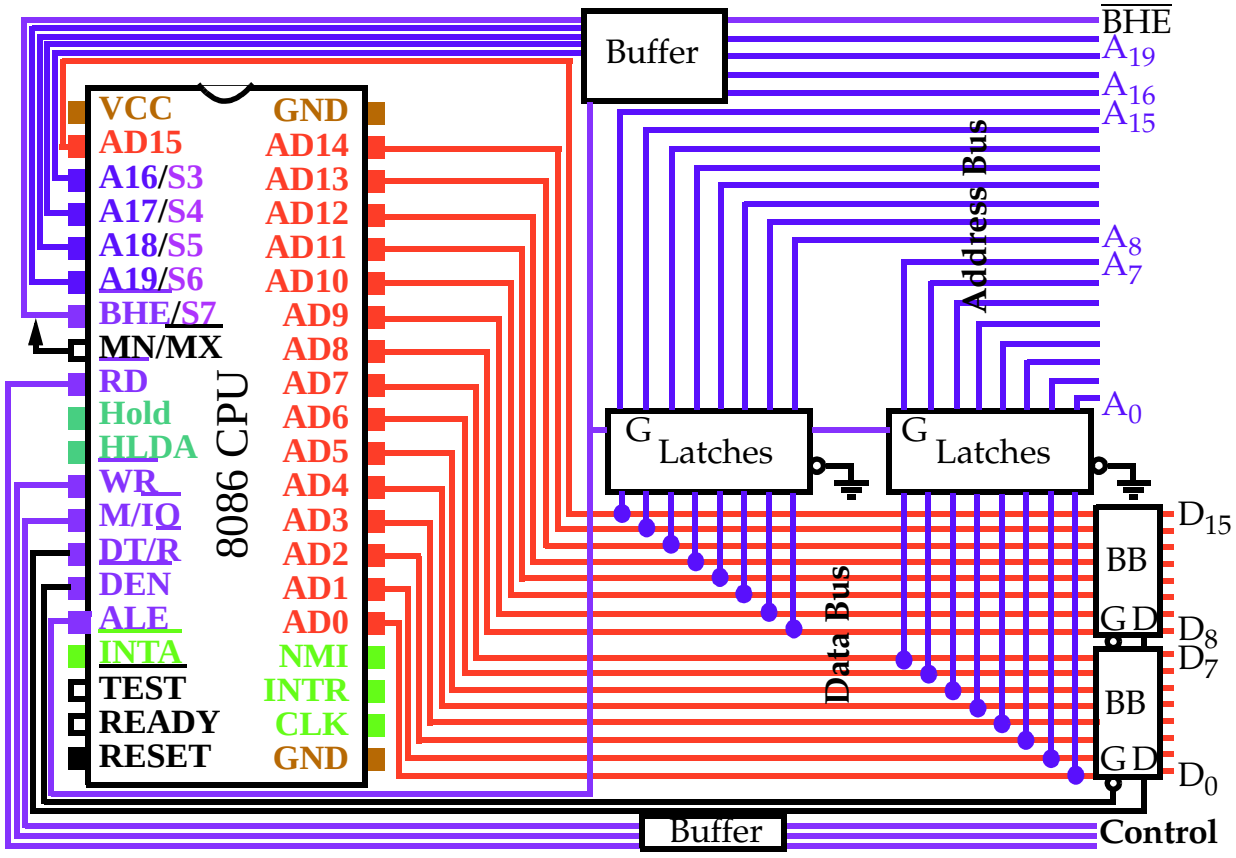
Final Exam

Name:

This exam is 12 pages long and has 4 questions and 1 extra credit question worth 15 points.

You must show all of your work -- partial credit may be given to partially correct answers, while answers with no justification may not receive full points. Use the back of the exam sheets if you need extra space.

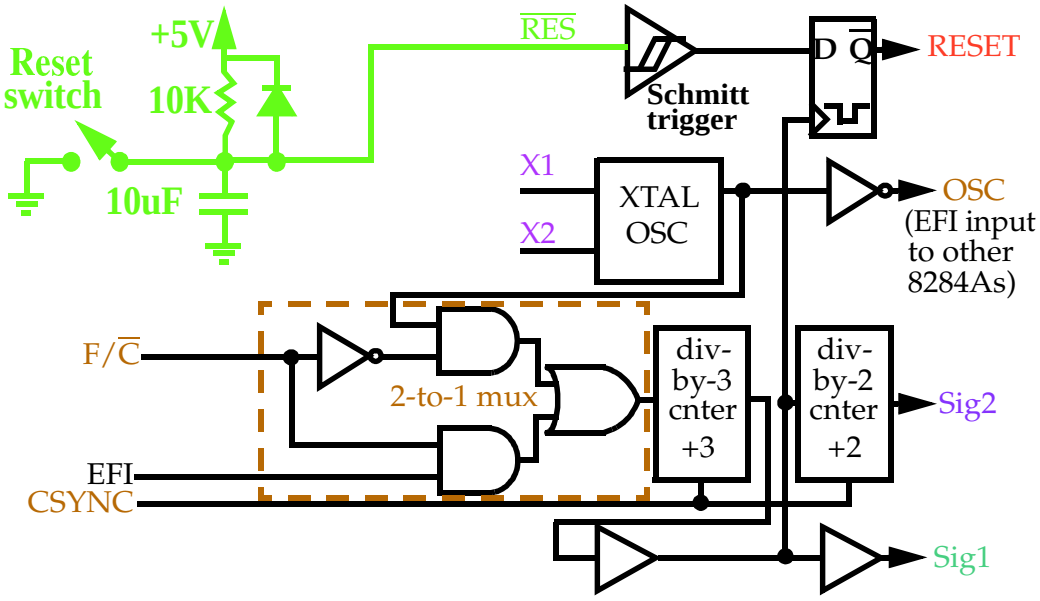
1) (9pts) a) The $\overline{DEN}$ (Data Bus Enable), DT/$\overline{R}$ (Data Transmit/Receive) and ALE (Address Latch Enable) pins of the 8086 are used to control the bus. Describe in words the sequence of events (steps) along with the values of these signals when reading and writing memory.



Read sequence: $\overline{DEN}$: DT/$\overline{R}$: ALE:

Write sequence: $\overline{DEN}$: DT/$\overline{R}$: ALE:

1) (8pts) b) Shown below is a portion of the schematic diagram for the 8284A Clock Generator chip.



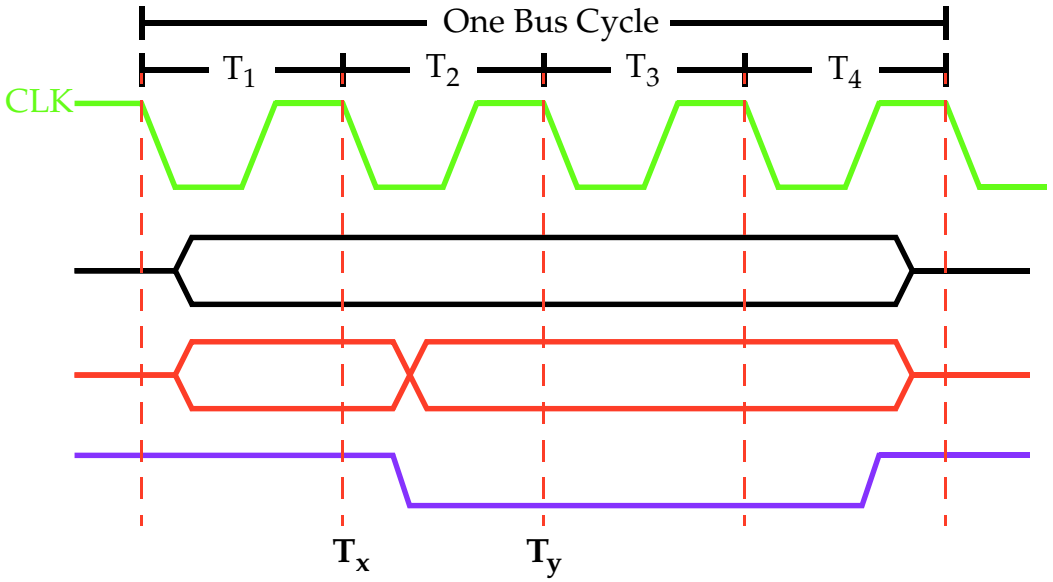
If X1 and X2 are driven externally by a 15MHz crystal, what are the frequencies of Sig1 and Sig2?

What are these outputs (Sig1 and Sig2) used to drive?

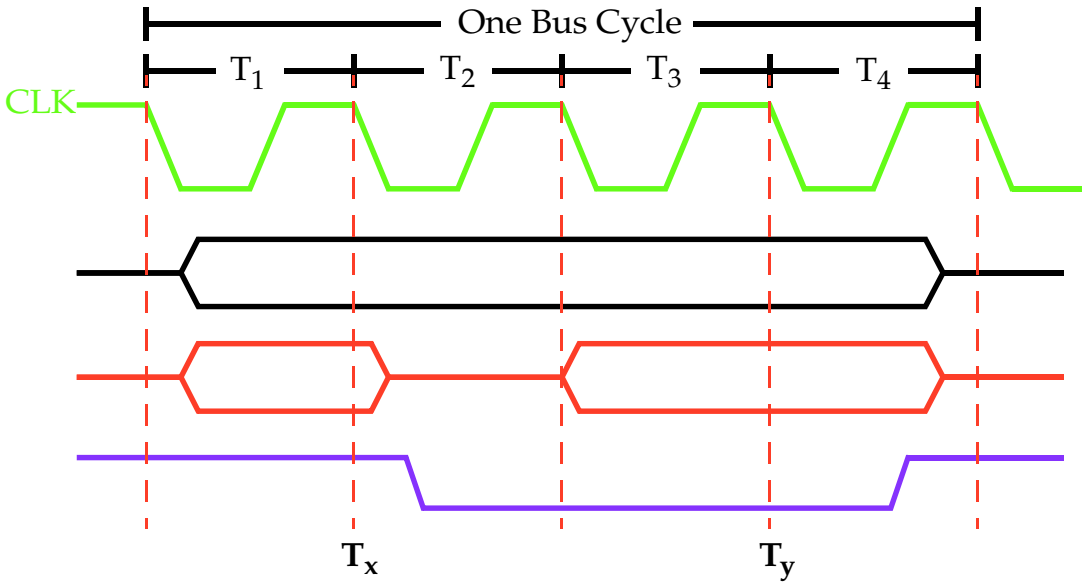
What is the purpose of the RC network on the $\overline{RES}$ signal?

Why is RESET driven from a negative edge-triggered D-flipflop?

1) (8pts) c) Label the following timing diagrams as a read or write processor/memory transaction. Label the diagram with the information on the bus (data or address) and the briefly describe the bus transaction (if any) that occurs at or around the time periods identified as T_x and T_y in each diagram.



T_x:
T_y:

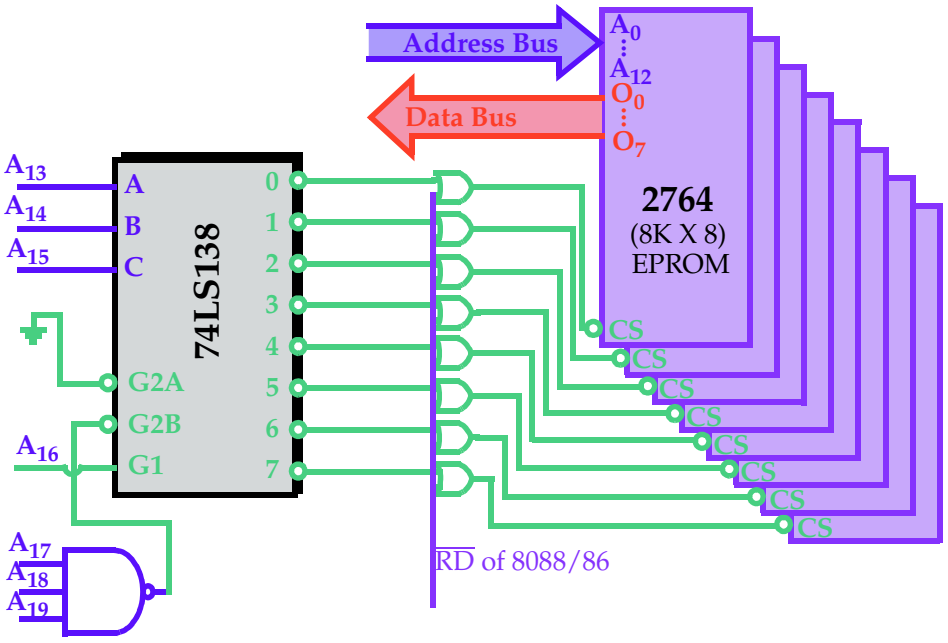


T_x:
T_y:

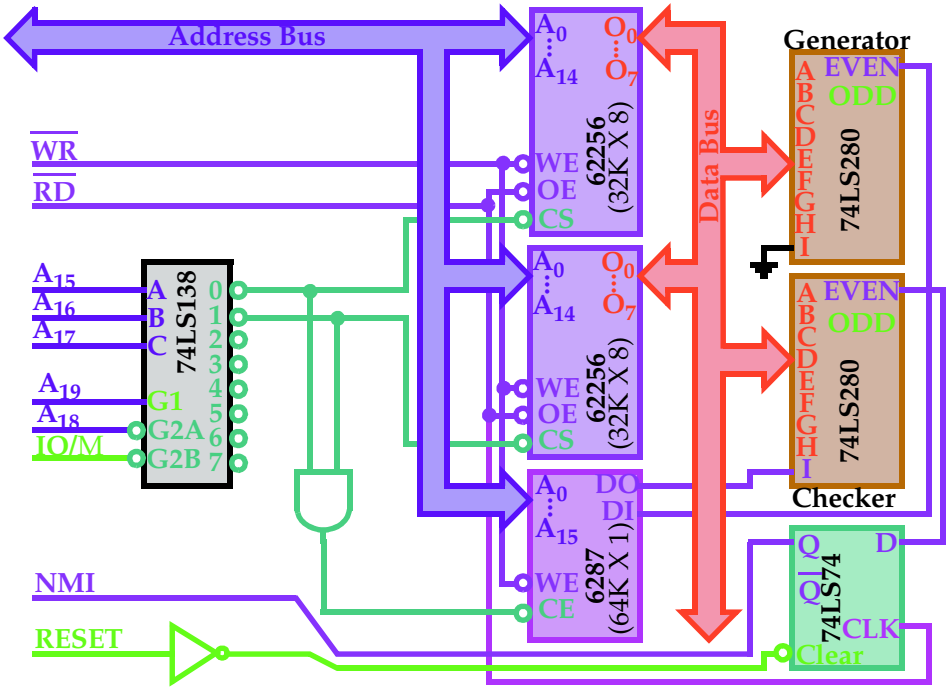
2) a) (3 pts) Name (do NOT explain) three types of erasable non-volatile read/write memories.

b) (3 pts) Why are DRAMs called dynamic RAM?

c) (5 pts) Give the range of addresses covered by each of the 8 outputs of the 3-to-8 line decoder.



2) d) (6 pts) Briefly explain how parity is generated and then checked in the following memory system.



e) (4 pts) Briefly explain (one sentence each) two other commonly used schemes to perform error detection.

2) f) (4 pts) Hamming codes can be used to perform single bit error correction. Given the following data byte, 11010010, compute the P_1 parity. Note that the four parity bits occupy subscript positions 1, 2, 4, and 8.

3) a) (4 pts) Describe two advantages of using modules over static compilation to install device drivers.

b) (4 pts) *insmod* is used to install modules. How is *insmod* similar to *ld* (the standard linker used for applications)? How is it different?

c) (4 pts) What are the purposes of the major and minor numbers associated with a device node in /dev?

d) (3 pts) Dynamic allocation of major numbers is accomplished by passing 0 as an argument to a function *register_chrdev*. What is the advantage of dynamically allocating major numbers?

3) e) (4 pts) Dynamic allocation of major numbers requires the device node in /dev to be created after the module is loaded. Briefly describe (in words) how this is may be accomplished using a script that creates the device node.

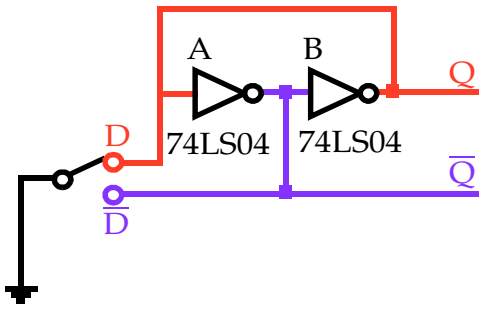
f) (2 pts) What are the two hardware resources that a device driver may need to acquire?

g) (4 pts) What are the two primary purposes of an interrupt service handler? Why is it not possible for the handler to transfer data directly to user space?

4) (4 pts) a) Name the basic component used to interface an input device to the bus of a microprocessor. Name the basic component used to interface an output device.

b) (4 pts) Briefly explain the difference between polling and interrupt driven I/O.

c) (4 pts) Briefly explain how the following circuit eliminates the problems associated with the physical bounce associated with the operation of a mechanical switch.

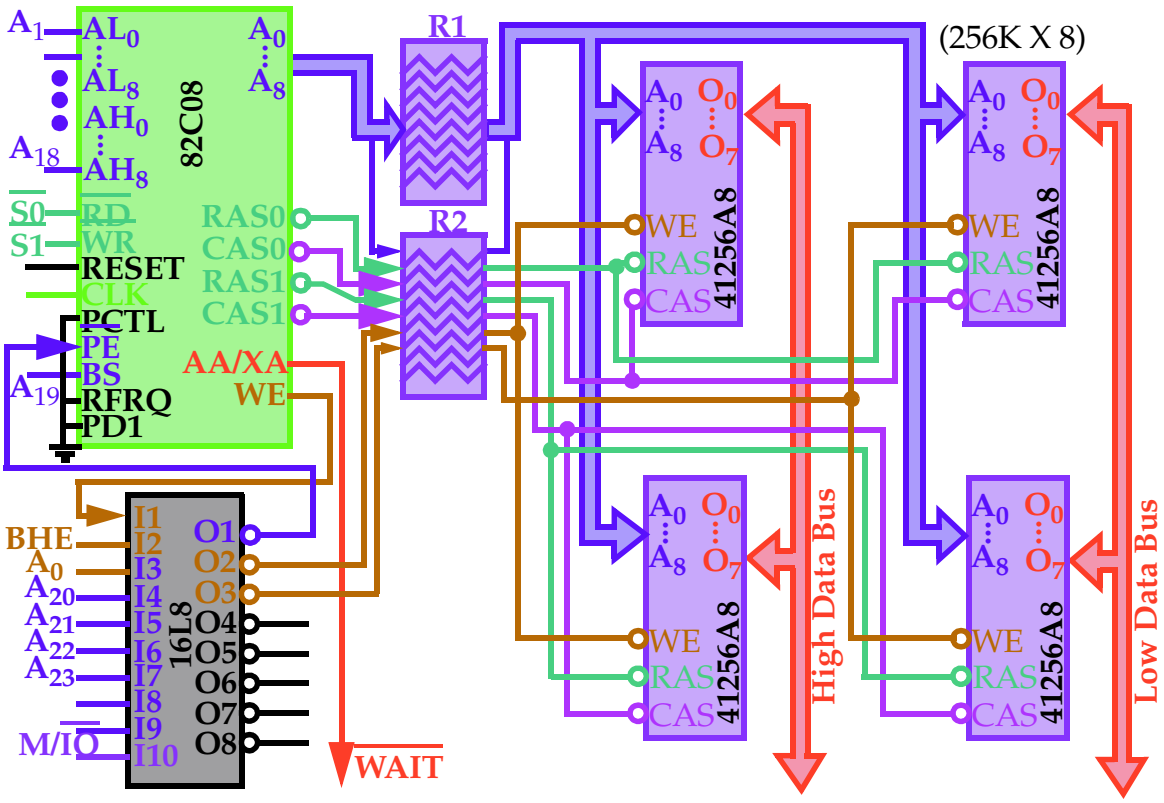


4) d) (4 pts) Name and briefly explain (one sentence) the pins dedicated to handling hardware interrupts on the 80x86.

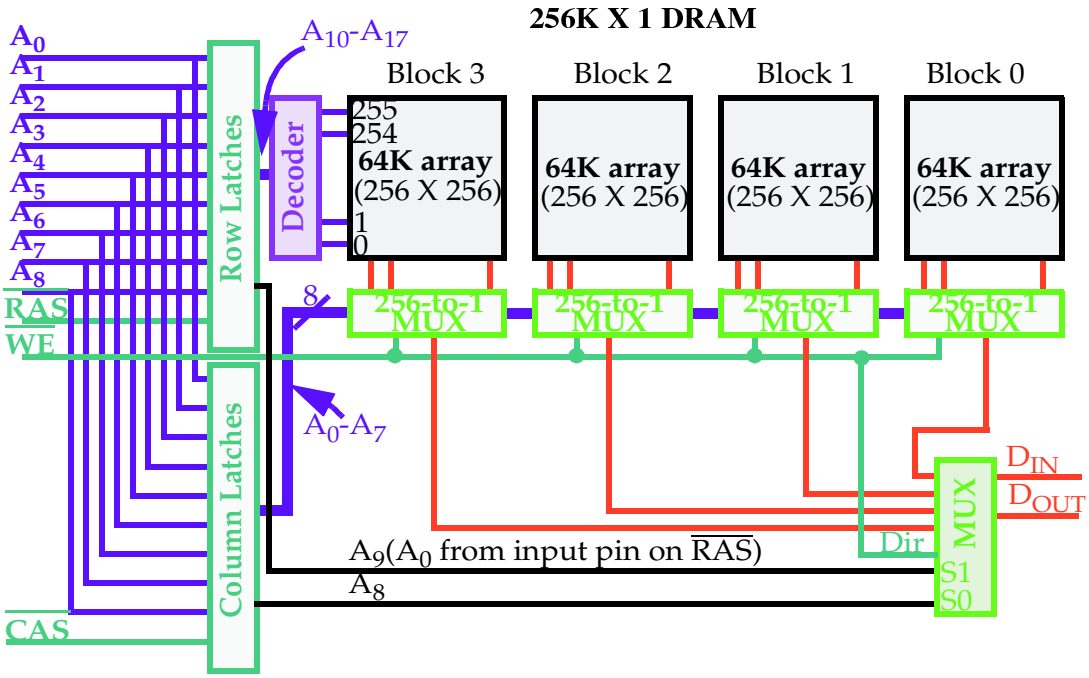
e) (4 pts) Name and briefly explain (one sentence) the four instructions that generate software interrupts on the 80x86.

f) (5 pts) Describe the sequence of events that occur when a software or hardware interrupt is generated.

5) (Extra Credit) (5 pts) a) Give the 16L8 program expressions required to control the three output signals O1 ($\overline{PE}$), O2 ($\overline{HWR}$) and O3 ($\overline{LWR}$) in the following memory system with DRAM controller.



b) (Extra Credit) (5 pts) Briefly explain the decoding operation that is performed for each of the $\overline{RAS}$ and $\overline{CAS}$ strobes.



c) (Extra Credit) (5 pts) Define EDO and SDRAM and briefly describe the performance advantage that each offers over conventional DRAM.