

ECE 238

Computer Logic Design

Overview

Course Catalog Description:

Topics include Binary number systems. Boolean algebra. Combinational, sequential, and register transfer logic. VHDL. Arithmetic/Logic unit. Memories, computer organization. Input-output. Microprocessors.

Prerequisites: C- or better in ECE 131

Textbook:

M. Morris Mano and Charles R. Kime, *Logic and Computer Design Fundamentals*, Prentice-Hall, 4th edition 2008, ISBN: 013198926X

Class Goals:

1. Understanding Boolean algebra and binary number systems, including binary, hexadecimal and octal.
2. Development of combinational and sequential logic design techniques at the gate and medium-scale integration (MSI) level. Using Boolean algebra and truth tables for combinational circuit analysis and design and state transition techniques for sequential circuits.
3. Exposure to VHDL as a tool for digital design, Knowledge of and hands on experience with FPGAs. Upon completion of this course, students should be able to design moderately complex digital circuits using these techniques.

Course Coordinator: Prof. Marios Pattichis

Table I: Objectives, Implementation, and Assessment

Objectives		Implementation	Assessment	A	B	C	D	E	F	G	H	I	J	K
O ₁	Understand digital computer systems and binary, octal, and hexadecimal number systems and arithmetic operations	3.75 hrs. lecture in 1 st two weeks	HW 1 Exam I	X				X						
O ₂	Understand basic gate circuit design and cost optimization. Use Boolean algebra and Karnaugh map as cost minimization techniques	7.5 hrs. lecture in week 2-4	HW 2-3 Exam I	X				X						
O ₃	Understand contemporary logic design process. Mastery of the practical combinational logic circuit design technique using functional building blocks	6.25 hrs. lecture in weeks 5-7	HW 4 Exam I	X		X		X						X
O ₄	Understand how arithmetic functions are implemented in modern computer using iterative design technique	2.5 hrs. lecture in week 8	HW 5, Exam II	X		X		X						X
O ₅	Understand modern design process for sequential circuit. Mastery of sequential circuit analysis and design technique using state machine diagram and state table formulation	8.75 hrs. lecture in weeks 9-12	HW6 Exam II	X		X		X						X
O ₆	Understand timing, pitfall and trade-offs (speed vs. cost) associated with implementations of gates, combinational and sequential circuits.	5 hrs lecture in week 13-14	HW7 Final Exam					X					X	X
O ₇	Understand modern multi-function register design technique - Register Transfer Level design	5 hrs lecture in week 15-16	HW8 Final Exam	X		X		X						X

O ₈	Basic experience with implementing hardware circuit design using VHDL programming on FPGAs to solve practical engineering problems	Lab lectures in weeks 1-16, VHDL homework Labs	VHDL HW 1-2 Labs 1-9	X	X	X		X		X				X	X
----------------	--	--	----------------------------	---	---	---	--	---	--	---	--	--	--	---	---

Table II: Expectation and Assessment Outcome
Fall 2008,
Dr. Honggang Yu

General expectations:

Homework:

These assignments involve two parts

1. Regular class homework aimed at helping students understand and master the basic computer logic circuit analysis and design technique. All the students are expected to be able to answer at least 85% of the problems assigned.
2. VHDL homework aimed at providing an introduction to VHDL syntax, programming structure and different VHDL design approaches. All the students are expected to be able to answer at least 95% of the problems assigned.

Lab Projects

Nine lab projects aimed at providing hands on VHDL programming experience in hardware design and verification. The students are expected to be able to use Xilinx ISE tools to design, synthesis, simulate and implement the circuit using CPLD and FPGA. 95% of the students are expected to be able to complete all the lab projects.

Exams:

Three exams total. Expect 70% of the students to score 70% or better on all exams.

Objectives		Outcome assessment	Evaluation
O ₁	Understand digital computer systems and binary, octal, and hexadecimal number systems and arithmetic operations	100% students completed 82.52% of exercise in HW 1. Av g. on Exam I was 66.68%. 55% of the students score 70% or better on Exam I	Time pressure in the exam affected the scores on Exam I.
O ₂	Understand basic gate circuit design and cost optimization. Use Boolean algebra and Karnaugh map as cost minimization techniques	100% students completed 85.95% of exercise in HW 2 and 81.56% in HW3. Av g. on Exam I was 66.68%. 55% of the students score 70% or better on Exam I	

O ₃	Understand contemporary logic design process. Mastery of the practical combinational logic circuit design technique using functional building blocks	100% students completed 78.2% of exercise in HW 4. Av g. on Exam I was 66.68%. 55% of the students score 70% or better on Exam I	
O ₄	Understand how arithmetic functions are implemented in modern computer using iterative design technique		
O ₅	Understand modern design process for sequential circuit. Mastery of sequential circuit analysis and design technique using state machine diagram and state table formulation		
O ₆	Understand timing, pitfall and trade-offs (speed vs. cost) associated with implementations of gates, combinational and sequential circuits.		
O ₇	Understand modern multi-function register design technique - Register Transfer Level design		
O ₈	Basic experience with implementing hardware circuit design using VHDL programming on FPGAs to solve practical engineering problems	97.5% students completed 100% of exercise in VHDL HW 1. 98% students complete lab1-5 projects.	

Course Schedule Fall 2008

Week	Date	Lect.	Topic	Assignment
1	26 Aug	1	Digital System Introduction & Course Administration	
	28 Aug	2	Binary, Octal, Hexadecimal Number System and Conversion	Ch. 1
2	02 Sep	3	1's and 2's Complements, Unsigned and Signed numbers	Ch. 1
	04 Sep	4	Unsigned and Signed numbers Arithmetic Operations and Coding,	Ch. 1
3	09 Sep	5	Introduction to Logic Gates and Boolean Algebra	Ch. 2
	11 Sep	6	Boolean Functions and their implementation, Canonical and Standard Forms	Ch. 2
4	16 Sep	7	K-Map Optimization and Multi-level Optimization	Ch. 2
	18 Sep	8	Don't Care States, Universal gates, Technology Mapping	Ch. 2
5	23 Sep	9	Combinational Circuits Analysis & Design Procedure	Ch. 3
	25 Sep	10	Decoders, Encoders, Priority Encoders	Ch. 3
6	30 Sep	11	Multiplexers / Demultiplexers	Ch. 3
	02 Oct	12	Binary Adder/Subtractor, Binary Multipliers	Ch. 4
7	07 Oct	13	Overflow detector and Design Applications	Ch. 4
	09 Oct	–	Exam I	
8	14 Oct	14	Introduction to Sequential Circuits, Latches, Flip Flops	Ch. 5
	16 Oct	–	<u>Fall Break</u>	
9	21 Oct	15	Types of Flip Flops	Ch. 5
	24 Oct	16	Sequential Circuit Analysis, State diagrams and State tables	Ch. 5
10	28 Oct	17	Sequential Circuit Design Procedure	Ch. 5
	30 Oct	18	Graphical state machine diagram model	Ch. 5
11	04 Nov	19	Sequential circuit timing analysis	Ch. 6
	06 Nov	20	Synchronous circuit pitfalls and asynchronous sequential circuit	Ch. 6
12	11 Nov	21	Registers, Shift Registers, Loading Registers, Serial/Parallel Registers,	Ch. 7
	13 Nov	22	Counters, Ripple Counters, Synchronous Binary Counters	Ch. 7
13	18 Nov	23	Register Transfer Level, Multi-function Register Design	Ch. 7
	20 Nov	–	Exam II	
14	25 Nov	24	ROM, PLA Devices, RAM	Ch. 6,8
	27 Nov	–	<u>Thanksgiving Holiday</u>	
15	02 Dec	25	Static and Dynamic RAM, Array of RAM ICs	Ch 8
	04 Dec	26	Array of RAM ICs	Ch 8
16	09 Dec	27	Memory construction using RAM Integrated Circuits	Ch 8
	11 Dec	28	Final Exam	