ELECTRONICS –I

Course Catalog Description: Introduction to diodes, bipolar, and field-effect transistors. Analysis, and design of digital circuits, gates, flip-flops and memory circuits. Circuits employing operational amplifiers. Analog to digital and digital to analog converters.
Prerequisites: C- or better in 213
Textbook: Segura and Hawkins, Digital CMOS Electronics (Book in preparation)
Class Goals: To provide the students with the basics of digital electronics starting from analyzing the operation of a field effect transistor to the simulation, layout and fabrication of digital logic circuits for combinational and sequential logic applications.
Course Coordinator: Prof. Sanjay Krishna

Table 1: Learning Outcomes, Implementation, and Assessment

Learning Outcomes		Implementation	Assessment	A	B	C	D	E	F	G	H	I	J	K
1	Analyze the process of band-formation in semiconductors and predict the behavior of electrons and holes in a p-n junction	2 Lectures	HW#1 Midterm 1 Final Exam	√	√			√			√	√	√	√
2	Analyze the operation of a field effect transistor and determine the DC/AC response of the FET	2 Lectures	HW#2 Midterm 1 Final Exam	√	√	√		√			√	√	√	√
3	Analyze the operation of a field effect transistor and determine the DC/AC response of the FET	2 Lectures	HW#3 Midterm 1 Final Exam	√	√			√			√	√	√	√
4	Design and analyze the operation of the CMOS Inverter, NAND, NOR, and T-gates	4 Lectures	HW#4, HW#5 Midterm 1 Final Exam Design Project	√		√	√	√	√	√	√	√	√	√
5	Determine the layout diagram for various logic gates	5 Lectures	HW#6, HW#7 Midterm 2 Final Exam Design Project	√		√	√	√	√	√	√	√	√	√
6	Draw the fabrication steps for fabrication of logic gate circuits	2 Lectures	HW#8 Midterm 2 Final Exam	√	√			√			√	√	√	√

7	Analyze memory and combinational logic circuit using sequential timing	4 Lectures	HW#9, HW#10 Midterm 2 Final Exam	√	√	√		√			√	√	√	√
8	Determine the best type of interconnect scheme for a given process	2 Lectures	HW#11 Final Exam	√	√			√			√	√	√	√
9	Work together in a team and evaluate/assess your individual performance and the performance of your teammates	2 Lectures	HW#12 Final Exam	√	√			√			√	√	√	√

Table II: Expectation and Assessment Outcome
Fall 2008, Instructor: Marek Osinski

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General expectations:
Homeworks:

Design Projects:

Exams: Expect 75% of the students to score 70% or better on all exams. (MAREK, PLEASE CHANGE ACCORDINGLY)

Objectives		Outcome Assessment	Evaluation
O_1	Understand basic analytical tools necessary for rigorous study of data structures and algorithms	87.5 % of students completed 100% of exercise in HW 1 & 2. Av g. on Exam I was 57.3%, with 53% scoring 70% or better	Some students lacked some prerequisite knowledge in discrete mathematics (Math 327).
O_2	Understand particular algorithmic design techniques	73% of the students completed HW 3 satisfactorily. Av g. on Exam I was 57.3%, with 53% scoring 70% or better	
O_3	Understand fundamental object-oriented (OO) design and programming concepts	100% of the students completed HW 4 satisfactorily. Av g. on Exam II was 57.6%, with 75% scoring 70% or better	Students lacked some prerequisite knowledge from the previous programming course in this sequence (ECE 231).
O_4	Understand how OO concepts are implemented in modern programming languages	93% of the students completed HW 5 satisfactorily. Av g. on Exam II was 57.6%, with 75% scoring 70% or better Avg of 68% on Project 1, 61% on Project 2, and 47% on Project 3.	Time constraints (end of semester) affected the scores on Project 3.
O_5	Understand trade-offs associated with implementations of various Dynamic Set ADTs	Avg of 68% on Project 1, 61% on Project 2, and 47% on Project 3. Av g. on Exam I was 59.1%, with 83% scoring 70% or better	
O_6	Gain experience implementing data structures and algorithms, and using these to solve practical engineering problems	Avg of 68% on Project 1, 61% on Project 2, and 47% on Project 3.	Project 1 – Discrete Fourier Transform in C Project 2 – Discrete Fourier Transform in C++ w/ applications to filtering Project 3 – Experimental Analysis of Data Structures

COURSE SCHEDULE-EECE 321- SPRING 2007
INSTRUCTOR: Sanjay Krishna (Marek, Replace with your schedule)

ECE-321 Electronics 1 ; COURSE OUTLINE Spring 2007			Tentative	
Lec#	Date	Topic	Reading Assignment	HW
1	Jan. 17	Introduction: Logic theory review, circuits review	Chap. 1	
2	Jan. 19	Introduction: circuits review, C, L, diode circuits	Chap. 1	
3	Jan. 22	Diode circuits	Chap. 1	HW1 Assigned
4	Jan. 24	Semiconductor Physics	Chap. 2	
5	Jan. 26	Semiconductor Physics	Chap. 2	
6	Jan. 29	Semiconductor Physics	Chap. 2	HW1 Due
7	Jan. 31	MOSFETS (Transistors) How does it Work	Chap. 3	
8	Feb. 2	MOSFETS (Transistors) *n* MOSFETs	Chap. 3	
9	Feb. 5	MOSFETS (Transistors) *n* MOSFETs	Chap. 3	HW2 Due
10	Feb. 7	MOSFETS (Transistors) *n* MOSFETs	Chap. 3	
11	Feb. 9	MOSFETS (Transistors)	Chap. 3	
12	Feb. 12	MOSFETS (Transistors), REVIEW		HW3 Due
13	Feb. 14	Mid Term I		
14	Feb. 16	MOSFETS (Transistors) Parasitic Capacitance, Scaling	Chap 3	
15	Feb. 19	CMOS Inverter	Chap. 4	HW4 Due
16	Feb. 21	CMOS Inverter	Chap. 4	
17	Feb. 23	CMOS Inverter	Chap. 4	
18	Feb. 26	CMOS Inverter	Chap. 4	HW5 Due
19	Feb. 28	CMOS Inverter	Chap. 4	
20	Mar. 2	CMOS Inverter	Chap. 4	
21	Mar. 5	CMOS Inverter (Instructor on Travel)	Chap. 4	HW6 Due
22	Mar. 7	Combinational Logic Synthesis	Chap. 5	
23	Mar. 9	Combinational Logic Synthesis	Chap. 5	
	Mar. 12th-16th	**** Spring Break ****	*No Class*	
24	Mar. 19	Combinational Logic Synthesis	Chap. 5	HW7 Due
25	Mar. 21	Combinational Logic Synthesis	Chap. 5	
26	Mar. 23	Combinational Logic Synthesis	Chap. 5	
27	Mar. 26	HW problems and exam review		HW8 Due
28	Mar. 28	Mid Term II		
29	Mar. 30	CMOS Layout and Design Rules	Chap. 6	
30	Apr. 2	CMOS Layout and Design Rules	Chap. 6	HW9 Due
31	Apr. 4	CMOS Layout and Design Rules	Handout	
32	Apr. 6	CMOS Layout and Design Rules	Chap. 5, 1-10	
33	Apr. 9	CMOS Fabrication	Chap. 8	HW10 Due
34	Apr. 11	CMOS Fabrication	Chap. 8	
35	Apr. 13	CMOS Fabrication	Chap. 8	
36	Apr. 16	Sequential Logic	Chap. 9	HW11 Due
37	Apr. 18	Sequential Logic	Chap. 9	
38	Apr. 20	Sequential Logic	Chap. 9	
39	Apr. 23	Intel Tour		HW12 Due
40	Apr. 25	Sequential Logic	Chap. 9	
41	Apr. 27	Interconnection Characteristics	Chap 7	
42	Apr. 30	Interconnection Characteristics	Chap 7	HW13 Due
43	May 2	Interconnection Characteristics	Chap 7	
44	4-May	Review Class		
	9th May	Final Exam (10:00AM-12:00PM)		