

ECE 338 Intermediate Logic Design

Course Catalog Description: Advanced combinational circuits; XOR and transmission gates; computer-based optimization methods; RTL and HDL; introduction to computer aided design; advanced sequential machines; asynchronous sequential machines; timing issues; memory and memory interfacing; programmable logic devices; VLSI concepts.

Prerequisites: C- or better in ECE 238L.

Textbook: Mano, M. M. & C. R. Kime, *Logic and Computer Design Fundamentals, 4th edition*, Englewood Cliffs, NJ: Prentice Hall, 2008. (later chapters)

Class Goals: This course delves deeper into logic design techniques than the introductory course (ECE 238) and provides students with experience in related areas – use of computer aided design tools and fundamentals of large programmable logic systems. The logic areas covered include complex arithmetic functions, error detecting/correcting methods, hand-shaking protocols, advanced sequential machines, asynchronous sequential systems, and related technology and implementation issues.

Course Coordinator: Prof. Howard Pollard

Table 1: Objectives, Implementation, and Assessment

Objectives-Sub objectives		Implementation	Assessment	A	B	C	D	E	F	G	H	I	J	K
O ₁	Develop skills in schematic capture and simulation systems	2.5 hour – weeks 1-2	Proj #1							✓		✓	✓	✓
O ₂	Develop ability to utilize VHDL for representing digital systems and simulating their behavior	5 hours – weeks 1-3	Proj #1 Exam #1, Final		✓	✓	✓	✓		✓		✓	✓	✓
O ₃	Understand use of and limits to representation of information with binary patterns	4 hours – weeks 2-4	Proj #1 Exam #1, Final	✓	✓	✓	✓			✓		✓		
O ₄	Understand algorithms for high speed combinational arithmetic – add/subtract, multiply and divide	6 hours – weeks 3-5	Proj #1 Exam #1, Final	✓	✓	✓								
O ₅	Understand algorithms for sequential arithmetic operations – multiply and divide	6 hours – weeks 6-7	Proj #2 Exam #2, Final	✓	✓	✓								
O ₆	Develop abilities to utilize RTL to describe transfers required to do work in digital systems	1.5 hours – weeks 7-8	Proj #2 Exam #2, Final		✓	✓	✓	✓						
O ₇	Understand different methods for implementing clocked sequential systems	6 hours – weeks 8-10	Proj #2 Exam #2, Final		✓	✓								
O ₈	Develop ability to create and analyze asynchronous sequential systems	6 hours – weeks 11-15	Proj #3 Exam #2, Final		✓									
O ₉	Understand technology issues related to implementation of digital systems – tri-state logic, timing issues, hazards	3 hours – weeks 13-14	Proj #2,3 Exam #2, Final	✓		✓	✓	✓					✓	✓
O ₁₀	Develop ability to implement memory systems with read only and read-write technologies	3 hours – weeks 14-16	Proj #2 Exam #2, Final											
O ₁₁	Understand mapping of logic systems on programmable logic devices	2 hours – weeks 3 & 16	Exam #2, Final	✓	✓	✓		✓				✓		

Table II: Expectation and Assessment Outcome

General expectation:

Projects(3): Expect 80% of students to complete all projects with grade of 80% or better.

Exams(2hr+final): Expect 70% of students to complete exams with grade of 65% or better.

Objectives-Subobjectives		Outcomes Assessment (% Success)		Evaluation
		Projects	Exams	
O ₁	Develop skills in schematic capture and simulation systems			
O ₂	Develop ability to utilize VHDL for representing digital systems and simulating their behavior			
O ₃	Understand use of and limits to representation of information with binary patterns			
O ₄	Understand algorithms for high speed combinational arithmetic – add/subtract, multiply and divide			
O ₅	Understand algorithms for sequential arithmetic operations – multiply and divide			
O ₆	Develop abilities to utilize RTL to describe transfers required to do work in digital systems			
O ₇	Understand different methods for implementing clocked sequential systems			
O ₈	Develop ability to create and analyze asynchronous sequential systems			
O ₉	Understand technology issues related to implementation of digital systems – tri-state logic, timing issues, hazards			
O ₁₀	Develop ability to implement memory systems with read only and read-write technologies			
O ₁₁	Understand mapping of logic systems on programmable logic devices			