

University of New Mexico Computer Design

Overview

Course Catalog Description: Computer architecture; design and implementation at HDL level; ALU, exception handling and interrupts; addressing; memory; speed issues; pipelining; microprogramming; introduction to distributed and parallel processing; buses; bus protocols, and bus masters. CAD project to include written and oral presentations.

Prerequisites: Electronics I, Computer Architecture and Organization, Microprocessors, and Intermediate Logic Design

Textbook: D. Patterson and J. Hennessy, *Computer Organization and Design, Fourth Edition – The Hardware/Software Interface*, Morgan Kaufman, 2009; supplements from additional texts for VHDL information and additional architecture information.

Class Goals: This course gives an in-depth understanding of the inner-workings of modern digital computer systems and tradeoffs present at the hardware-software interface. The student will get an understanding of the design process in the context of a complex hardware system, gain practical experience with computer-aided design tools, and learn how to work in groups.

Course Coordinator: Prof. L. Howard Pollard

Table 1: Objectives, Implementation, and Assessment

Objectives-Subobjectives		Implementation	Assessment	A	B	C	D	E	F	G	H	I	J	K
O ₁	Understand basic computer organization	1.25 hour lecture in week 1	Proj #1,#3 Exam 1	✓	✓			✓			✓	✓	✓	
O ₂	Evaluate performance of computer systems using simple models	1.25 hours – week 1	Proj #3, Exam 2	✓	✓			✓	✓		✓		✓	
O ₃	Design simple instruction set	3 hours – weeks 3-6	Proj #3 Exam 2	✓	✓	✓		✓						✓
O ₄	Design of arithmetic and logic units	4.5 hours – weeks 2-4	Proj #1, Exam 1	✓		✓		✓						✓
O ₅	Design of processor datapath and control	8 hours – weeks 6-11	Proj #2,#3 Exam 2, 3	✓	✓	✓		✓					✓	✓
O ₆	Design of pipelined datapath and control	3.5 hours – weeks 7-11	Proj #3 Exam 2, 3	✓		✓		✓					✓	✓
O ₇	Understand concepts of superscalar processor design	2 hours – weeks 8,12	Exam 3	✓	✓			✓		✓			✓	✓
O ₈	Understand memory organization: cache and virtual memory systems	4 hours – weeks 12-13	Proj #3, Exam 2, 3	✓	✓			✓		✓			✓	✓
O ₉	Design simple interfaces of processors with peripherals	4 hours – weeks 13-14	Proj #3 Exam 2, 3	✓	✓			✓		✓				✓
O ₁₀	Have a feel for advanced concepts in computer system design	4 hours – weeks 14-16	Exam 3	✓	✓			✓		✓		✓	✓	✓

Table II: Expectation and Assessment Outcome

General expectations:

Projects: Expect 85% of students to complete all three projects with grade of 80% or better

Exams: Expect 75% of students to complete all exams with grade of 70% or better

Objectives-Subobjectives		Outcomes Assessment (% Success)		Evaluation
		Projects	Exams	
O ₁	Understand basic computer organization			
O ₂	Evaluate performance of computer systems using simple models			
O ₃	Design simple instruction set			
O ₄	Design of arithmetic and logic units			
O ₅	Design of processor datapath and control			
O ₆	Design of pipelined datapath and control			
O ₇	Understand concepts of superscalar processor design			
O ₈	Understand memory organization: cache and virtual memory systems			
O ₉	Design simple interfaces of processors with peripherals			
O ₁₀	Have a feel for advanced concepts in computer system design			