

ECE 337

Introduction to Computer Architecture and Organization

Overview

Course Catalog Description:

Survey of various levels of computer architecture and design: microprogramming and processor architecture, advanced assembly language programming, operating system concepts, and input/output via the operating system.

Prerequisites: C- or better in 238, either 231 or CS241L

Textbook:

Structured Computer Organization, Andrew S. Tanenbaum, Fifth Edition
ISBN: 0131485210, Prentice Hall

Class Goals:

Architecture is the many layers of software, firmware, and hardware, which work together to provide the programmer with a productive development environment and convenient abstractions for the complex and detailed interfaces. This course presents various levels of computer architecture and design. The students are expected to

1. Understand the important components of a computer system, and how these components are interrelated.
2. Understand how high level functionalities are supported by the hardware.
3. Knowledge about the nature and characteristics of modern computer systems.

Course Coordinator: Prof. Marios Pattichis

O ₈	Understand the relationship of higher level, abstract ideas to the features of a machine's architecture. Understand how different architectures affect computer system performance	lectures in weeks 1-16, Class project	Class Project Final Exam	X	X	X		X		X			X	X
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Table II: Expectation and Assessment Outcome
Fall 2008,
Dr. Honggang Yu

General expectations:

Homework

Regular class homework aimed at helping students understand and master the basic computer system architecture levels and organization structures. All the students are expected to be able to answer at least 90% of the problems assigned.

Pop-up Quizzes

Pop-up Quizzes aimed at checking the basic computer architecture knowledge of the students in time. The contents of the quizzes are strongly based on class lectures and homework problems. All the students are expected to be able to complete 80% of the questions.

Exams:

One midterm exam and one final exam. Expect 80% of the students to score 80% or better on all exams.

Term Paper

Each student is required to work independently on a term paper for this course. A term paper is a research report of a specific architectural problem that a student might be interested in. Each student is asked to present his/her term paper in class.

Objectives		Outcome assessment	Evaluation
O ₁	Understand the concepts and techniques of constructing machines as a series of levels (Multilevel Machines)	87.5 % of students completed 100% of exercise in HW 1. Av g. on Exam I was 82.63%	
O ₂	Understand the CPU instruction execution cycle, CISC and RISC architectures	100% students completed 90% of exercise in HW 2. Av g. on Quiz 1 was 68.33%. Av g. on Exam I was 82.63%	Some students didn't review class materials in time and prepare for the pop-up quiz

O ₃	Understand the components of a computer system, and how these components are interrelated.	100% students completed 90% of exercise in HW 3. Av g. on Quiz 2 was 66.07%. Av g. on Exam I was 82.63%	
O ₄	Understand the design of memory, data path, control store, and design of microprograms	100% students completed 90% of exercise in HW 4. Av g. on Quiz 3 was 60.71%. Av g. on Exam I was 82.63%	
O ₅	Understand cache architectures, branch predictions and scheduling of multiple instruction issue		
O ₆	Understand instruction set level architecture and design principles		
O ₇	Understand parallel computer configurations, shared-memory and message-passing multicomputers etc.		
O ₈	Understand the relationship of higher level, abstract ideas to the features of a machine's architecture. Understand how different architectures affect computer system performance		

Course Schedule Fall 2008

Week	Date	Lect.	Topic	Assignment
1	25 Aug	1	Introduction & Course Administration	
	27 Aug	2	Contemporary Multilevel computer machine	Ch. 1
	29 Aug	3	History of computer architecture development and categories	Ch. 1
2	01 Sep	4	Computer systems and components	Ch. 2
	03 Sep	5	CPU organization and instruction execution	Ch. 2
	05 Sep	6	RISC vs CISC and Parallel Processing	Ch. 2
3	08 Sep	7	Primary memory	Ch. 2
	10 Sep	8	Secondary memory	Ch. 2
	12 Sep	9	Inputs/Outputs devices	Ch. 2
4	15 Sep	10	Review of Basic Gates, Combinational and Sequential Circuit	Ch. 3
	17 Sep	11	Review of Boolean Algebra and Arithmetic Circuits	Ch. 3
	19 Sep	12	Registers, Memory Organization and chips	Ch. 3
5	22 Sep	13	CPU and modern CPU chip examples	Ch. 3
	24 Sep	14	Buses and modern buses examples	Ch. 3
	26 Sep	15	I/O chips and address decoding	Ch. 3
6	29 Sep	16	Introduction of the microarchitecture level	Ch. 4
	01 Oct	17	The data Path of Mic-1	Ch. 4
	03 Oct	18	The control store of Mic-1 and microinstructions	Ch. 4
7	06 Oct	19	The example ISA level, IJVM	Ch. 4
	08 Oct	20	The IJVM Instruction set	Ch. 4
	10 Oct	21	Implementation of IJVM using Mic-1 (1)	Ch. 4
8	12 Oct	22	Implementation of IJVM using Mic-1 (2)	Ch. 4
	15 Oct	–	Midterm Exam	
	17 Oct	–	<i>Fall Break</i>	
9	20 Oct	23	Design principles of the microarchitecture level	Ch. 4
	22 Oct	24	Mic-2 Microarchitecture level	Ch. 4
	24 Oct	25	Mic-3 Microarchitecture level	Ch. 4
10	27 Oct	26	Mic-4 Microarchitecture level	Ch. 4
	29 Oct	27	Cache memory	Ch. 4
	31 Oct	28	Branch Prediction	Ch. 4
11	03 Nov	29	Out-of-order Execution and register renaming	Ch. 4
	05 Nov	30	Speculative execution	Ch. 4
	07 Nov	31	Examples of the microarchitecture level	Ch. 4
12	10 Nov	32	Overview of the ISA level	Ch. 5
	12 Nov	33	Data types in ISA level	Ch. 5
	14 Nov	34	Instruction formats in ISA level	Ch. 5
13	17 Nov	35	Addressing mode	Ch. 5
	19 Nov	36	Instruction types in ISA level	Ch. 5
	21 Nov	37	Flow of control and recursion	Ch. 5
14	24 Nov	38	The IA-64 architecture (1)	Ch. 5

	26 Nov	39	The IA-64 architecture (2)	Ch. 5
	28 Nov	–	<u>Thanksgiving Holiday</u>	
15	01 Dec	40	On-chip parallelism	Ch 8
	03 Dec	41	coprocessors	Ch 8
	05 Dec	42	shared-memory multiprocessors	Ch 8
16	08 Dec	43	message-passing multicomputers	Ch 8
	10 Dec	44	Grid computing	Ch 8
	12 Dec	–	Final Exam	