

# ECE 238 Exam 1

Name Solution 5

Problem 1 15 /15

Problem 2 30/30

Problem 3 40/40

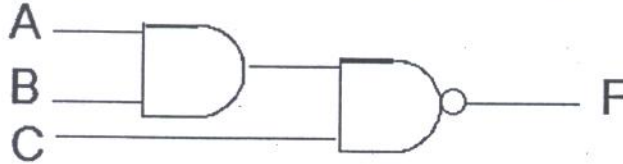
Problem 4 15 /15

Total 100 /100

**Good Luck!**

**Problem 1 (15 points)**

In the circuit given below, we want to apply the **transport delay** model to compute the output  $F$  and the output of the AND and NAND gates for a given set of inputs. Note that for the transport-delay model, we do not need to worry about the rejection time. We only need to know the propagation delay. Assume that the propagation delay is 1 nano-second.



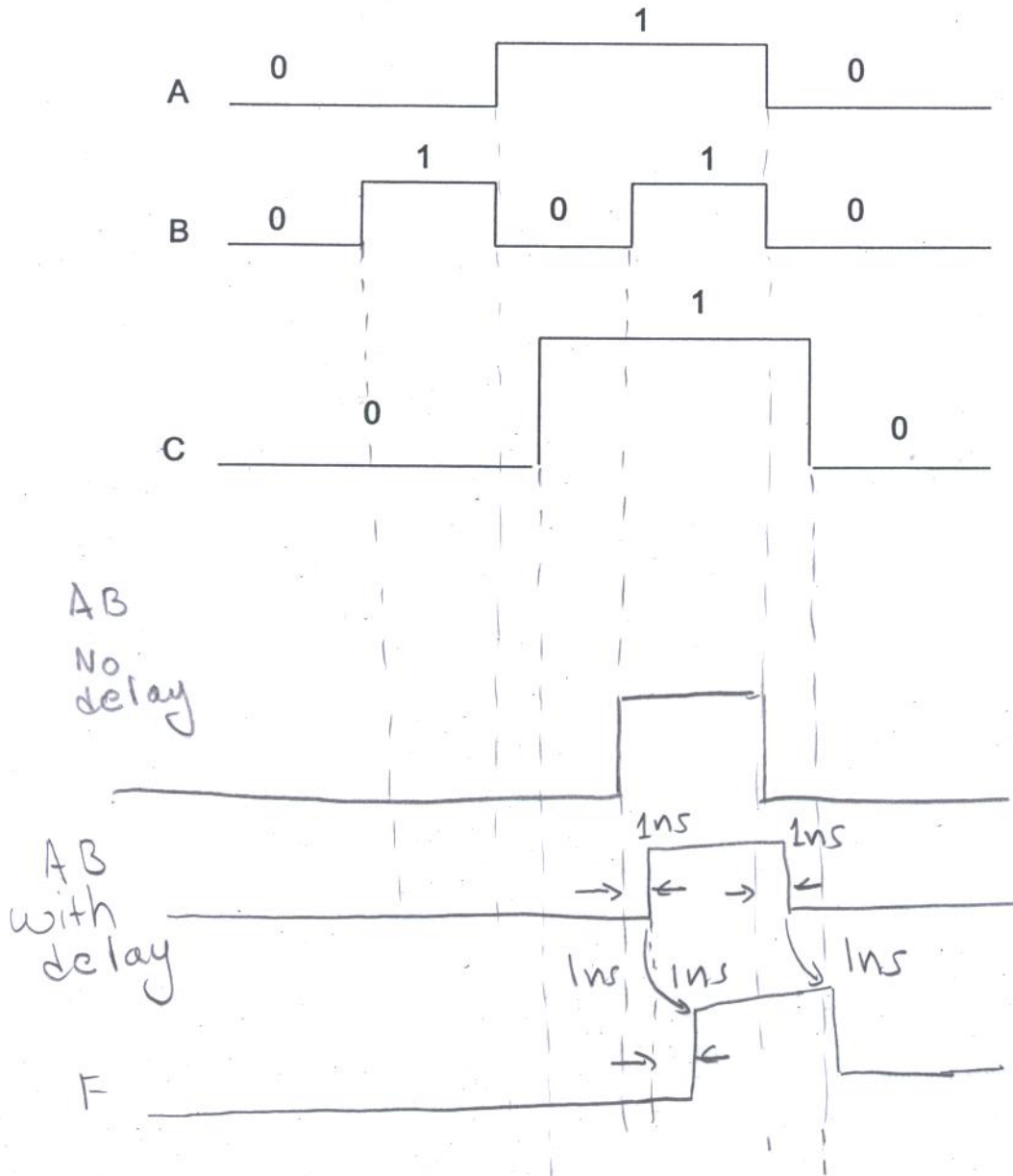
1(a)(2 points) Give an expression for  $F$  as a function of  $A, B, C$ .

$$F = ((AB) \cdot C)' = A' + B' + C'$$

1(b)(3 points) Construct a truth table to show the output  $F$  for all possible input combinations.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

1(c)(10 points) Assuming that the inputs  $A, B, C$  are changing as given below. Please compute the output of the AND-gate and  $F$ . Assume that the width of the pulse for which  $A$  stays high is 3 nano-seconds. Please indicate how the transportation delay is used in determining the outputs.



**Problem 2(30 points) VHDL**

In this problem, consider the VHDL code given below.

```
library IEEE;
use IEEE.std_logic_1164.all;

entity Comb_eg is port (IN_0,IN_1,IN_2,IN_3: in STD_LOGIC;
                       OUT_0: out STD_LOGIC);
end Comb_eg;

architecture Comb_eg is
  signal And_1_to_Inv_1, And_2_to_Or1, Inv_1_to_Or_1: STD_LOGIC;

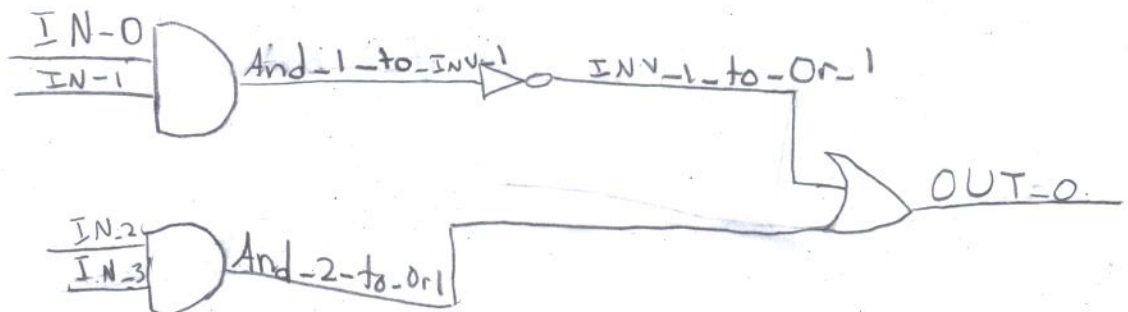
  component inv port (I: in STD_LOGIC; O: out STD_LOGIC);
  end component;

  component and2 port (IN_0, IN_1: in STD_LOGIC; OUT_0: out STD_LOGIC);
  end component;

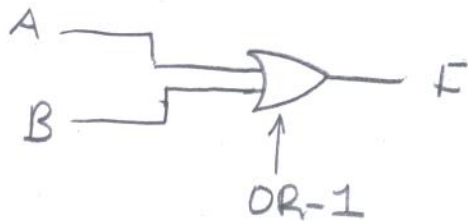
  component or2 port (IN_0,IN_1: in STD_LOGIC; OUT_0: out STD_LOGIC);
  end component;

begin
  Inv_1: inv port map (And_1_to_Inv_1, Inv_1_to_Or_1);
  And_1: and2 port map (IN_0, IN_1, And_1_to_Inv_1);
  And_2: and2 port map (IN_2, IN_3, And_2_to_Or1);
  Or_1: or2 port map (Inv_1_to_Or_1, And_2_to_Or1, OUT_0);
end Comb_eg;
```

**2(a)(15 points)** Draw the actual circuit that is represented by the VHDL code. Make sure to label all the signals.



2(b)(15 points) Draw and label the circuit  $F = A + B$ . Then, provide all the VHDL code for implementing this circuit.



```
library IEEE;
use IEEE.std_logic_1164.all;

entity My-CKT is port (A,B:in STD_LOGIC;
                      F:out STD_LOGIC);
end My-CKT is
component or2 port (IN_0,IN_1:in STD_LOGIC;
                  OUT_0:out STD_LOGIC);
end component
begin
Or_1: or2 port map (A,B,F);
end My-CKT;
```

**Problem 3 (40 points).**

In what follows, we want to implement  $f(A) = A - 2$  for three-bit inputs. Please read the instructions carefully and answer each part separately.

3(a)(3 points) For the inputs, we want to use three-bit **signed numbers**  $(a_2a_1a_0)_2$ . Give all the numbers that can be represented using three bits. Here, assume that we are using the two's complement representation for representing negative numbers.

$a_2$	$a_1$	$a_0$	$A$
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

3(b)(6 points) Plug in all numbers represented in 3(a) into  $f(A) = A - 2$  and derive the outputs bits.

$A$	$f(A) = A - 2$
0	-2
1	-1
2	0
3	1
-4	-6
-3	-5
-2	-4
-1	-3

3(c)(2 points) Based on your result in 3(b), how many bits do we need in order to represent the result?

$N$  bits:  $-2^{n-1} \rightarrow 2^{n-1} - 1$

4 bits:  $-8 \rightarrow 7$

4 bits needed

OK!

3(d)(10 points) Provide a truth table where the input is  $A = (a_2 a_1 a_0)_2$  and the output is  $f(A) = A - 2 = (O_n O_{n-1} \dots O_0)_2$ , where  $n$  is determined from your answer in 3(c).

IN			OUT $f(A) = A - 2$			
$a_2$	$a_1$	$a_0$	$O_3$	$O_2$	$O_1$	$O_0$
0	0	0	1	1	1	0
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	1	0	0	0	1
1	0	0	1	0	1	0
1	0	1	1	0	1	1
1	1	0	1	1	0	0
1	1	1	1	1	0	1

3(e)(14 points) Use three-variable Karnaugh maps to determine minimum sums of products for each one of  $(O_n O_{n-1} \dots O_0)_2$ .

$O_3: a_1 a_0$

	$a_2$	00	01	11	10
0	1	1	0	0	0
1	1	1	1	1	1

$O_3 = \bar{a}_1 + a_2$

$O_2: a_1 a_0$

	$a_2$	00	01	11	10
0	1	1	0	0	0
1	0	0	1	1	1

$O_2 = \bar{a}_2 \bar{a}_1 + a_2 a_1$

$O_1: a_1 a_0$

	$a_2$	00	01	11	10
0	1	1	0	0	0
1	1	1	0	0	0

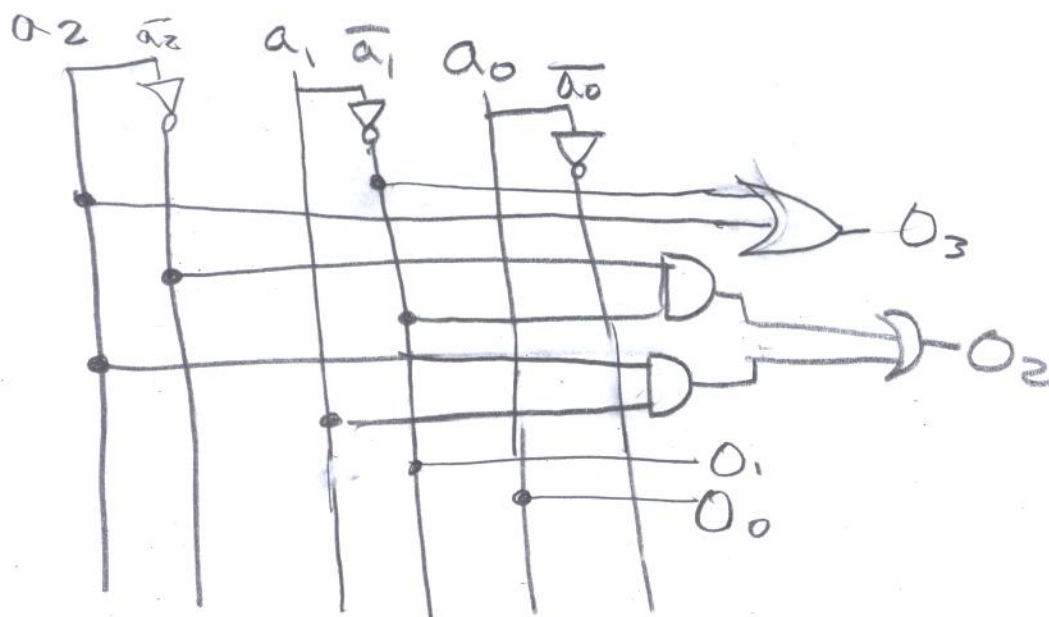
$O_1 = \bar{a}_1$

$O_0: a_1 a_0$

	$a_2$	00	01	11	10
0	0	1	1	0	0
1	0	1	1	0	0

$O_0 = a_0$

3(f)(5 points) Show the circuits for realizing  $(O_n O_{n-1} \dots O_0)_2$  based on your answer from 3(e).



**Problem 4(15 points)**

4(a) Give the minimum *sum of products* and minimum *product of sums* for:

$$F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 7, 9), \text{ with don't cares } m(11, 12).$$

4(b) Show the circuit realization for the sum of products.

4(c) Show the circuit realization for the product of sums.

4(d) Implement the circuit using a 4 to 1 multiplexer and any additional gates.

4(a)

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	X
1	1	0	0	X
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

$F_{00} = 1$   
 $F_{01}$   
 $F_{10} = D$   
 $F_{11} = 0$

F:

AB \ CD	00	01	11	10
00	1	1	1	1*
01	1	0	1	0
11	X	0	0	0
10	0	*1	X	0

$$F = B'D + A'B' + A'CD + \begin{cases} AC'D \\ BC'D \end{cases} \text{ or Min SOP}$$

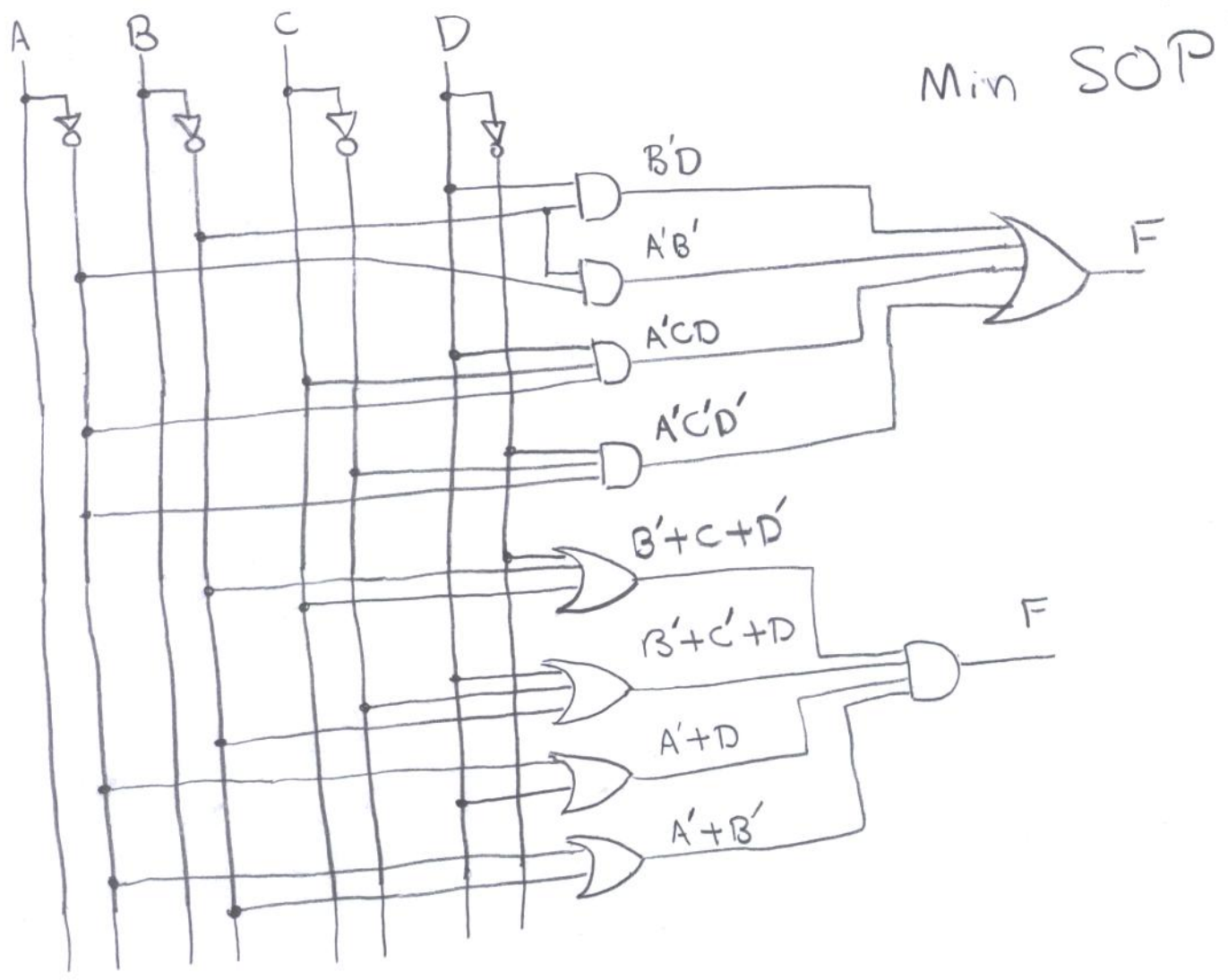
F':

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	1*	0	*1
11	X	1	1	1
10	1	0	X	1

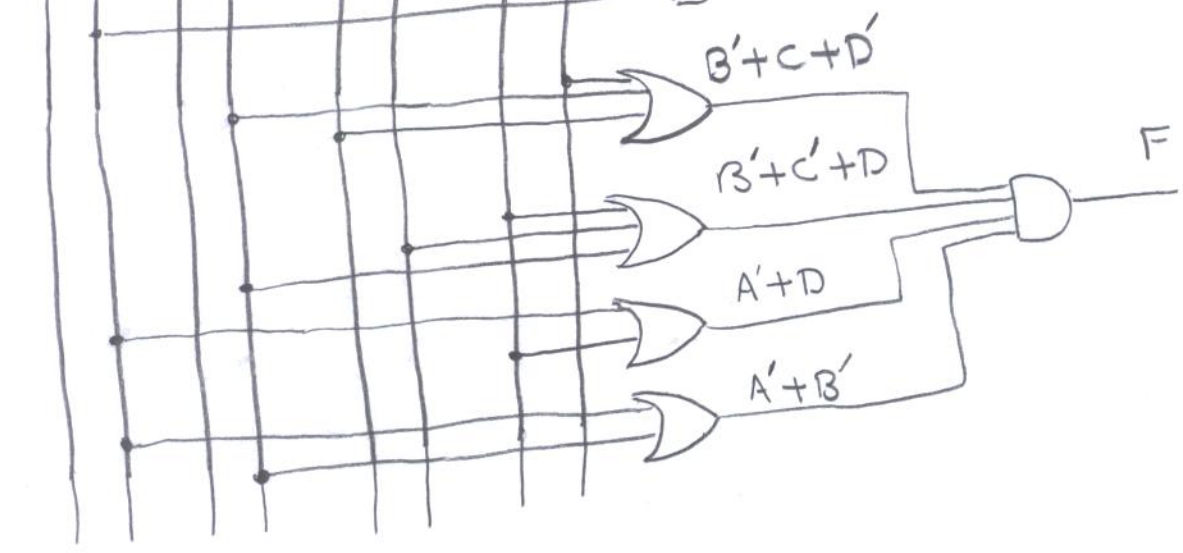
$$F' = C'DB + BCD' + \begin{cases} AB + AD' \\ AC + AD' \end{cases}$$

$$\Rightarrow F = (C + D' + B') \cdot (B' + C' + D) \cdot (A' + D) \cdot \begin{cases} (A' + B') \\ (A' + C') \text{ or} \end{cases}$$

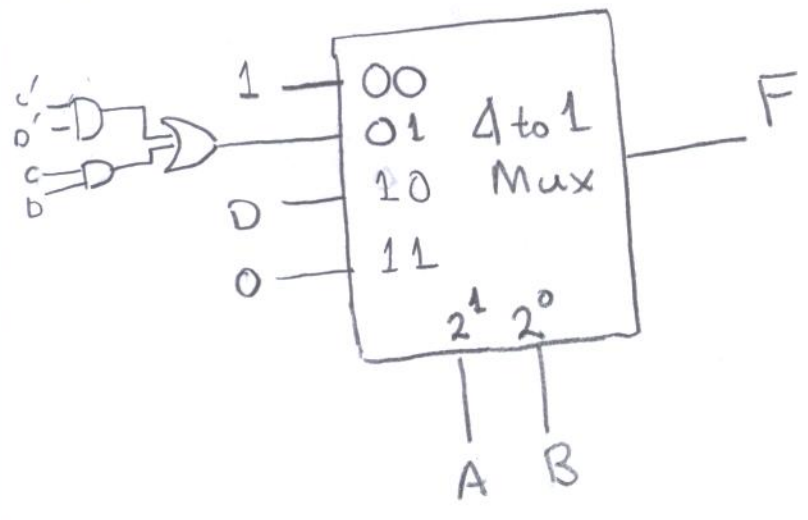
4(b)



4(c)



4(d)



		D	
	C	0	1
C	0	1	0
	1	0	1

$$F_{01} = C'D + CD$$