Jim Plusquellic

ECE Department, University of New Mexico
MSC01 1100, 1 University of New Mexico
Albuquerque, NM 87131-0001
Office: 505-277-0785, Cell: 240-475-1882, FAX: 505-277-1349
jimp@ece.unm.edu, http://www.ece.unm.edu/faculty/jimp/

Education

Ph.D.	1997	University of Pittsburgh, Computer Science
M.S.	1995	University of Pittsburgh, Computer Science
B.S.	1983	Indiana University of Pennsylvania, Biology

Work Experience

2008-present	Associate Professor, ECE Dept., Univ. of New Mexico
2003-2008	Associate Professor, CSEE Dept., Univ. of Maryland, Baltimore County
2006	NASA Faculty Fellowship Program, NASA, Goddard (June-Aug.)
2003-2004	Sabbatical at IBM Austin Research Laboratory (Sept.-May) and National Institute of Standards and Technology (June-Aug.)
1997-2002	Assistant Professor, Univ. of Maryland, Baltimore County
1989-1997	Graduate student, Univ. of Pittsburgh, PA
1985-1989	Air Quality Services, Pittsburgh, Gas and Liquid Chromatography

Honors and Awards

- *Invited Talk*, Intel FSM College of Engineering, Technical Seminar Series, March 2013
- **Golden Core Award**, IEEE Computer Society, Jan. 2013
- *Invited Participant*, "Convergence of Software Assurance Methodologies and Trustworthy Semiconductor Design and Manufacture", Sponsored by NSF, SRC and CCC, Jan. 15-16, 2013
- **Outstanding Contribution Award**, IEEE Computer Society, "In Recognition as Co-Founder of and providing Outstanding Contributions to the IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) for the Past Four Years 2008-2012", June 3, 2012
- Awarded *Best IP Session for VTS 2011*, VLSI Test Symposium (VTS), Jan. 2012
- International Test Conference, *10 Years of Continuous Service Award*, Oct. 2011

- Appointed *TTTC Technical Activity Chair*: Hardware Security and Trust, Sept. 2011
- Appointed *Associate Editor*, Transactions on Computers, Feb. 2011
- Structural Tester Donation (Ocelot ZFP Tester) from Verigy, June 2010
- ***General Chair***, Hardware-Oriented Security and Trust, June 2010
- **Co-founder** of IEEE International Workshop on Hardware-Oriented Security and Trust (HOST), June, 2008 (with Mohammad Tehranipoor)
- *General Chair*, Defect-Based Testing Workshop, Oct. 2006
- International Test Conference, *5 Years of Continuous Service Award*, Oct. 2006
- VLSI Test Symposium *Best Paper Award*, May 2005
- ACM *Distinguished Service Award*, "For Exemplary Service to ACM/SIGDA and the Design Automation Conference as Director of the University Booth Program", June 2003
- *IBM Visiting Scholar*, Austin Center for Advanced Studies, IBM Austin Research Laboratory, June-July 2001
- Awarded 2001 and 2002 *Austin CAS Fellow Award*
- Awarded the *Pennsylvania Space Grant Consortium Fellowship*, Aug. 1995

Research Support

2011-2014	SHF: Small: Measurement and Analysis of Regional Process Variations using Existing and Minimally Invasive On-Chip Embedded Resources, $300,000, P.I.
2010-2013	ATE Project: Developing the Digital Technologist for the New Millennium, NSF, $700,000, Co-P.I.
2010-2013	TC: Small: Collaborative Research: Exploration and Validation of Hardware Primitives for Security and Trust , NSF, $361,342, P.I.
2007-2011	Detection and Isolation of Malicious Inclusions in Secure Hardware (DIMINISH), NSF, $150,000, P.I.
2007-2008	Controller Design for Time-to-Digital Conversion Time-of-Flight Chip, NASA, $13,000, P.I.
2007-ongoing	Embedded Test Structures for Variation Analysis, Access to IBM's 65 nm and 90 nm PDK, future funding opportunities, IBM ARL, P.I.
2006-2007	RF-ADC Chip Test Project, $30,000, NASA, Co-P.I.
2005-2006	RF-ADC Chip Design Project, $85,000, NASA, Co-P.I.
2004-2006	Defect Based Test for Detection and Localization, $20,000, IBM Faculty Partnership Award, P.I.

2003-2004	Power Supply Signal Analysis for Defect Detection, Fault Localization and Diagnosis, $40,000, IBM Faculty Partnership Award, P.I.
2001-2004	Production-Oriented V_{DDT} and I_{DDQ} Device Testing Methods Based on Multiple Power Supply Pad Measurements, $318,000, NSF, P.I.
2002-2003	Novel VLSI Testing and Diagnostics Methods for Silicon Technology, $40,000, IBM Faculty Partnership Award, P.I.
2002-2003	Hardware Verification of Novel Power Supply Defect Detection and Diagnosis (research chip fabrication grant), ~$10,000, NSF, P.I.
2001-2002	Multiple Power Supply Pad V_{DDT} Testing for Delay Faults, $25,000, IBM Faculty Partnership Award, P.I.
2001-2002	Dynamic Transport Selection for Mobile Computing, $50,000, Aether grant, Co-P.I.
2000-2001	Fitting Rovibronic Spectra with Genetic Algorithms, $10,000, NIST grant, P.I.
2000-2001	Multiple Power Supply Pad V_{DDT} Testing for Delay Faults, $25,000, IBM Faculty Partnership Award, P.I.
2000-2001	Simulator to Evaluate/Prototype Local Area and Personal Area Wireless Network Protocols and Products, $80,000, Aether grant, Co-P.I.
1999-2000	Power Supply Transient Signal Analysis for Defect Detection using the FISHNET ASIC, $74,194, DOD, P.I.

Pending Support

NSF, small and medium, 2013

Sabbaticals and Off-Site Work Experiences

NASA Faculty Fellowship Program, NASA, Goddard (June-Aug. 2006)

IBM Austin Research Laboratory, Sept. 2003-May 2004

National Institute of Standards and Technology (June-Aug. 2004)

Equipment and Chip Fabrication Donations

2011	**~$100K from Remington Test for 2 Micromanipulator 8860 Probe Stations**
2010	**~$400K from Verigy for Ocelot ZFP Tester**

2010	~$30K from MOSIS, MEP Research support program to build a chip in IBM's 10LPe (90 nm Low Power CMOS), Project Title: "Exploration of Validation of Hardware Primitives for Security and Trust"
2008	~$50K from AFRL, SemiProbe IC packaging instrument and PCB fabrication equipment including pick-and-place/re-flow oven.
2003-2004	~$80K from Tektronics for teaching laboratories
2003-2004	~$20K from Xilinx for teaching laboratories
2002-2003	$13,360, Intel equipment grant
2001-2002	$2,701, Xilinx FPGA/software grant
1999-2000	$17,808, Intel equipment grant
1999-2000	$12,500, DRIF award, UMBC
1997-1998	Lockheed Martin Faculty Development, $3,000, UMBC

Students

Current Ph.D. Students

Mitchell Martin

Fareena Saqib

Joshua Trujillo

Raj Chakraborty

Dylan Ismari

Ian Wilcox

Tony Maokhamphiou

Current MS Students

Bill Cavanaugh

Carlos Montoya

Ph.D. Degrees Awarded

Jing Ju, 2013, **chair**, Hunan University of Science and Technology

Jim Aarestad, 2013, **chair**, currently working for COSMIAC

Matthew Areno, 2013, **chair**, currently working for Sandia National Laboratory

Charles Lamech (w/ distinction), 2012, **chair**, joined Intel Corp.

Ryan Helinski (w/ distinction), 2010, **chair**, joined Sandia National Laboratory

Mikhail Itskovich, 2009, **chair**, joined Atmel

Dhruva Acharyya, 2008, **chair**, joined IBM ARL, now with Advantest Inc.

Reza MohammadPourrad, 2008, **chair**, research associate UNM, ST Micro

Tom Goff, 2006, member

Abhishek Singh, 2005, **chair**, joined NVidia

Xiao Lin, 2005, member

Chintan Patel, 2004, **chair**, assistant prof. UMBC

Eliza Yingzi Du, 2003, member

Naomi Avigdor, 2002, member

William Freeman, 2000, member

MS Degrees Awarded

John Vranes (project), July, 2013, member

Michael Basile (project), June, 2013, **chair**

Phani Kumar Kandregula (project), April, 2013, member

Joshua Trujillo (thesis), November, 2012, **chair**

Mike Echert (project), October, 2012, member

Kanamu Pupuhi (project), October, 2012, member

Tony Maokhamphiou (project), July, 2012, **chair**

Thomas LeBoeuf (project), November, 2011, member

Paco Maldonado (project), November, 2011, member

Mirza (project), November, 2011, member

Mitchell Martin (project), April, 2011, **chair**

Michael Thomas (thesis), April 2011, **chair**

Jim Aarestad (thesis), April 2011, **chair**

Naveen Purushotham (project), November, 2010, member

Shyam Kottaman (project), July, 2010, member

Fareena Saqib (thesis), May, 2010, member

Greg Feucht (thesis), April, 2010, **chair**

Andrea Wright (project), April, 2010, member

Soumik Banerjee (project), March, 2010, member

Srikanth ... (Nasir's student), December, 2009, member

Yang Song (project), November, 2009, member

Sev Shelley (thesis), November, 2009, member

Colby Hoffman (thesis), July, 2009, member

Jason R Hamlet (thesis), March, 2009, member

Ryan Helinski, (thesis), July, 2008, **chair**

Shiva Selvarajan, (thesis), June, 2008, **chair**

Joshua Lottich, (thesis), April, 2007, member

Li Deng (project), Jan. 2007, **chair**

Haricharan Kotagiri (thesis), Dec. 2006, member

Mahesh Balakristin (thesis), Sept. 2006, **chair**

Prasath Periyasamy (thesis), Aug. 2006, member

Mohammed ElShoukry (thesis), Aug. 2006, member

Pei Huang (project), Aug. 2006, **chair**

Hok Tang (thesis), Nov. 2005, member

Jitin Tharian (thesis), March 2005, **chair**

Pushkar Pulastya (thesis), Aug. 2004, **chair**

Junping Zhang (project), Dec. 2004, member

Smita Pawar (project), Aug. 2003, **chair**

Shanmugavel Ponnusamy (thesis), Nov. 2002, member

Sanat Kamal Bahl (thesis), Aug. 2002, **chair**

Abhishek Singh (thesis), Aug. 2002, **chair**

Chintan Patel (thesis), Aug. 2001, **chair**

Ying Ouyang (thesis), Aug. 2000, **chair**

Amy Germida (thesis), Jan. 2000, **chair**

Felix K. Watson (thesis), July 1999, member

Zheng Yan (project), Aug. 1999, **chair**

Chuan-Fu Lin (project), May 1999, **chair**

Krishnakamar Sivasankaran (thesis), Sept. 1998, member

Undergraduate Student Research

Thomas Bauer, Spring 2012, Tom will be designing a PCB for use in a prototype of an OpAmp based comparator scheme for a Physical Unclonable Function.

Ghadeh Hadi, Summer 2010, Ghadeh is helping with the design of a 65 nm chip using Cadence.

Ghadeh Hadi, Summer 2009, Ghadeh is working with my graduate students to setup our Integrated Circuit Hardware Analysis Laboratory (IC-HAL).

Ryan Helinski, Fall-Spring, 2006-07, Ryan is coding an ATPG algorithm to determine fault coverage for our small delay fault detection strategy.

Kory Schoenfliess, Spring and Summer 2003, TSMC 0.18um standard cell library.

Michael Riggs, Summer and Fall, 2002, Performance and area comparison of several CORDIC algorithms using FPGAs.

Johnathan Hudson, Ryan Robucci, Amir Rowhanirad, Ernesto Staroswiecki. Supervised these recipients of the 2001 Provost's Undergraduate Research Award for a entitled "Home Automation Implemented Using a Low-Cost Reconfigurable Hardware Module", UMBC Review, 2002. (Ryan is now a graduate student at Georgia Tech).

Jonathan Hudson, Summer 1999, Winter 2000, Summer 2000.

Ernesto Staroswiecki, Summer 1999, Summer 2000. (Ernesto spent the summer of 2003 as an intern at IBM's Austin Research Lab and is now a graduate student at Stanford).

Publications

Journal Publications

1. J. Aarestad, P. Ortiz, D. Acharyya and J. Plusquellic, "HELP: A Hardware-Embedded Delay-Based PUF", *Design and Test of Computers*, Vol. 30, Issue: 2, Mar., 2013. pp. 17-25.
2. M. Abramovici, D. Agarwal, S. Bhunia, P. Bradley, M. S. Hsiao, J. Plusquellic and M. Tehranipoor, "Protection against Hardware Trojan Attacks: Towards a Comprehensive Solution", Volume: PP , Issue: 99, *Design and Test of Computers*, 2012.
3. H. Salmani, M. Tehranipoor and J. Plusquellic, "A Novel Technique for Improving Hardware Trojan Detection and Reducing Trojan Activation Time", *Transactions on VLSI*, Volume: 20 , Issue: 1, 2012 , pp. 112-125.
4. C. Lamech, R. Rad, M. Tehranipoor and J. Plusquellic, "An Experimental Analysis of Power and Delay Signal-to-Noise Requirements for Detecting Trojans and Methods for Achieving the Required Detection Sensitivities" *Trans. Information Forensics and Security*, Volume: 6 , Issue: 3 , Part: 2, 2011, pp. 1170-1179.
5. J. Aarestad, D. Acharyya, R. Rad and J. Plusquellic, "Detecting Trojans Though Leakage Current Analysis Using Multiple Supply Pad I_{DDQ}s", *Transactions on Information Forensics and Security*, Volume: 5, Issue: 4, 2010, pp. 893-904.
6. R. M. Rad, M. Tehranipoor, J. Plusquellic, "A Sensitivity Analysis of Power Signal Methods for Detecting Hardware Trojans under Real Process and Environmental Conditions", *Transactions in VLSI*, Volume: 18, Issue: 12, 2010, pp. 1735-1744.
7. R. M. Rad, J. Plusquellic, "A Novel Fault Localization Technique Based on Deconvolution and Calibration of Power Pad Transients Signals", *Journal of*

Electronic Testing, Theory and Applications, Volume 25, Numbers 2-3, June 2009.

8. R. Helinski, J. Plusquellic, "Measuring Power Distribution System Resistance Variations", *Transactions on Semiconductor Manufacturing*, Volume 21, Issue 3, Aug. 2008, pp. 444-453.
9. J. Lee, M. Tehranipoor, C. Patel, J. Plusquellic, "Securing Designs Against Scan-Based Side-Channel Attacks", *Transactions on Dependable and Secure Computing*, Volume 4, Number 4, Oct.-Dec. 2007, pp. 325-336.
10. J. Plusquellic, D. Acharyya, A. Singh, M. Tehranipoor, C. Patel, "Quiescent-Signal Analysis: A Multiple Supply Pad I_{DDQ} Method", *Design and Test of Computers*, Volume 23, Issue 4, April 2006, pp. 278-293.
11. A. Singh, J. Plusquellic, D. Phatak, C. Patel, "Defect Simulation Methodology for iDDT Testing", *Journal of Electronic Testing, Theory and Applications*, Volume 22, Number 3, June 2006, pp. 255-272.
12. C. Patel, A. Singh, J. Plusquellic, "Defect Detection Using Quiescent Signal Analysis", *Journal of Electronic Testing, Theory and Applications*, Volume 21, Number 5, Oct. 2005, pp. 463-483.
13. S. Kamal Bahl, J. Plusquellic, J. Thomas, "A Comparative Study of W-CDMA Cell Search Designs", *Journal of Circuits, Systems and Computers*, Volume 14, Number 1, Feb. 2005, pp. 129-136.
14. C. Patel, E. Staroswiecki, S. Pawar, D. Acharyya, J. Plusquellic, "Defect Diagnosis using a Current Ratio based Quiescent Signal Analysis Model for Commercial Power Grids", *Journal of Electronic Testing, Theory and Applications*, Volume 19, Number 6, Dec. 2003, pp. 611-623.
15. D. S. Phatak, T. Goff, J. Plusquellic, "IP-in-IP Tunneling to Enable the Simultaneous use of Multiple IP Interfaces for Network Level Connection Striping", *Computer Networks: The International Journal of Computer and Telecommunications Networking*, Volume 43, Issue 6, Dec. 2003, pp. 787-804.
16. J. Plusquellic, A. Singh, C. Patel, A. Gattiker, "Power Supply Transient Signal Analysis for Defect-Oriented Test", *Transactions on Computer Aided Design of Integrated Circuits and Systems,* Volume 22, Issue 3, March 2003, pp. 370-374.
17. J. Plusquellic, "IC Diagnosis Using Multiple Supply Pad I_{DDQ}s", *Design and Test of Computers*, Volume 18, Number 1, Jan. 2001, pp. 50-61.
18. J. Plusquellic, D. M. Chiarulli, S. P. Levitan, "Time and Frequency Domain Transient Signal Analysis for Defect Detection in CMOS Digital ICs", *Transactions on Circuits and Systems I,* Volume 46, Issue 11, Nov. 1999, pp. 1390-1394.
19. J. Plusquellic, D. M. Chiarulli, S. P. Levitan, "Digital IC Device Testing by Transient Signal Analysis (TSA)", *Electronics Letters*, Volume 31, Issue 18, Aug. 1995, pp. 1568–1570.

Journal Papers: Unpublished

20. F. Saqib, A. Dutta, J. Plusquellic, P. Ortiz, M. S. Pattichis, "Pipelined Decision Tree Classification Accelerator Implementation in FPGA (DT-CAIF)", revising for *Trans. on Computers*, Oct. 2012.
21. F. Saqib, D. Ismari and J. Plusquellic, "Within-Die Delay Variation Measurement and Analysis Using An Embedded Test Structure", submitted *Trans. VLSI*, June, 2013.

Refereed Conference Publications

1. M. Areno and J. Plusquellic, "Secure Mobile Association and Data Protection with Enhanced Cryptographic Engines", accepted *PRISMS*, 2013.
2. J. Ju, C. Lamech, J. Plusquellic, "Stability Analysis of a Physical Unclonable Function based on Metal Resistance Variations", accepted *Symposium on Hardware-Oriented Security and Trust (HOST)*, 2013.
3. J. Aarestad, D. Acharyya, J. Plusquellic, "An Error-Tolerant Bit Generation Technique For Use With A Hardware-Embedded Path Delay PUF", accepted *Symposium on Hardware-Oriented Security and Trust (HOST)*, 2013.
4. R. Chakraborty, C. Lamech, D. Acharyya and J. Plusquellic, "A Transmission Gate Physical Unclonable Function and On-Chip Voltage-to-Digital Conversion Technique," accepted *Design Automation Conference*, 2013.
5. M. Areno and J. Plusquellic, "Securing Trusted Execution Environments with PUF Generated Secret Keys", *TrustCom*, 2012.
6. J. Ju, R. Chakraborty, R. Rad, J. Plusquellic, "Bit String Analysis of Physical Unclonable Functions based on Resistance Variations in Metals and Transistors", *Symposium on Hardware-Oriented Security and Trust (HOST)*, 2012, pp. 13-20.
7. C. Lamech and J. Plusquellic, "Trojan Detection based on Delay Variations Measured using a High-Precision, Low-Overhead Embedded Test Structure", *Symposium on Hardware-Oriented Security and Trust (HOST)*, 2012, pp. 75-82.
8. C. Lamech, J. Aarestad, J. Plusquellic, R. Rad, K. Agarwal, "REBEL and TDC: Two Embedded Test Structures for On-Chip Measurements of Within-Die Path Delay Variations", *International Conference on Computer-Aided Design (ICCAD)*, 2011, pp. 170-177.
9. C. Lamech, J. Aarestad, K. Agarwal, J. Plusquellic, "Characterizing Within-Die and Die-to-Die Delay Variations Introduced by Process Variations and SOI History Effect", *Design Automation Conference* (*DAC*), 2011, pp. 534-539.
10. J. Plusquellic, D. Acharyya, K. Agarwal, "Measuring Spatial Variation Profile through Power Supply Current Measurements", *International Symposium on Quality Electronic Design* (*ISQED*), 2011, pp. 1-5.
11. K. Agarwal and J. Plusquellic, "Minimally Invasive Methods for Characterizing Within-Die Variation", **(INVITED PAPER)** for Innovative IP

Practice session called On-Chip Parametric Sensors, *VLSI Test Symposium*, 2011.

12. D. Acharyya, K. Agarwal, J. Plusquellic, "Leveraging Existing Power Control Circuits and Power Delivery Architecture for Variability Measurement", *International Test Conference*, 2010.
13. J. Plusquellic and D. Acharyya, "Leveraging the Power Grid for Localizing Trojans and Defects", *International Symposium on Testing and Failure Analysis*, 2010.
14. R. Helinski, D. Acharyya, J. Plusquellic, "Quality Metric Evaluation of a Physical Unclonable Function Derived from an IC's Power Distribution System", *Design Automation Conference*, 2010, pp. 240-243.
15. V. Murray, G. A. Feucht, J. C. Lyke, M. Pattichis, J. Plusquellic, "Cell-Based Architecture for Reconfigurable Wiring Manifolds", *American Institute of Aeronautics and Astronautics*, 2010.
16. K. Agarwal, D. Acharyya, J. Plusquellic, "Characterizing Within-Die Variation from Multiple Supply Port I_{DDQ} Measurements", *International Conference on Computer-Aided Design*, 2009, pp. 418-424.
17. R. Helinski, D. Acharyya, J. Plusquellic, "A Physical Unclonable Function Defined Using Power Distribution System Equivalent Resistance Variations", *Design Automation Conference*, 2009, pp. 676 - 681.
18. R. M. Rad, X. Wang, M. Tehranipoor, J. Plusquellic, "Power Supply Signal Calibration Techniques for Improving Detection Resolution to Hardware Trojans", *International Conference on Computer-Aided Design*, Nov., 2008, pp. 632-639.
19. W. Xiaoxiao, S. Hassan Salmani, M. Tehranipoor, J. Plusquellic, "Hardware Trojan Detection and Isolation Using Current Integration and Localized Current Analysis", *International Symposium on Defect and Fault Tolerance in VLSI Systems*, Oct. 2008, pp. 87-95.
20. M. Itskovich, J. Plusquellic, "I_{DDT} Test Calibration Using a Programmable Processing Array", *4th Southern Conference on Programmable Logic*, March, 2008, pp. 265-268.
21. J. Plusquellic, D. Acharyya, M. Tehranipoor, C. Patel, "Triangulating to a Defect's Physical Coordinates Using Multiple Supply Pad IDDQs: Test Chip Results", *International Symposium on Testing and Failure Analysis*, Nov. 2006, pp. 36-45.
22. K. Agarwal, F. Liu, C. McDowell, S. Nassif, K. Nowka, M. Palmer, D. Acharyya, J. Plusquellic, "A Test Structure for Characterizing Local Device Mismatches", *Symposium on VLSI Circuits*, June 2006, pp. 67-68.
23. J. Lee, M. Tehranipoor, J. Plusquellic, "A Low-Cost Solution for Protecting IPs against Scan-Based Side-Channel Attacks", *VLSI Test Symposium*, May 2006, pp. 42-47.
24. N. Ahmed, C. P. Ravikumar, M. Tehranipoor, J. Plusquellic, "At-Speed

Transition Fault Testing with Low Speed Scan Enable", *VLSI Test Symposium*, May 2005, pp. 42-47 (**BEST PAPER AWARD**).

25. D. Acharyya, J. Plusquellic, "Hardware Results Demonstrating Defect Detection using Power Supply Signal Measurements", *VLSI Test Symposium*, May 2005, pp. 433-438.
26. J. Lee, M. Tehranipoor, C. Patel, J. Plusquellic, "Securing Scan Design Using Lock and Key Technique", *International Symposium on Defect and Fault Tolerance in VLSI Systems*, Oct. 2005, pp. 51-62.
27. D. Acharyya, J. Plusquellic, "Hardware Results Demonstrating Defect Localization using Power Supply Signal Measurements", *International Symposium on Testing and Failure Analysis*, Nov. 2004, pp. 58-66.
28. A. Singh, C. Patel, J. Plusquellic, "Fault Simulation Model for iDDT Testing: An Investigation", *VLSI Test Symposium*, April 2004, pp. 304-310.
29. A. Singh, C. Patel, J. Plusquellic, "On-chip Impulse Response Generation for Analog and Mixed-signal Testing", *International Test Conference*, Oct. 2004, pp. 262-270.
30. C. Patel, A. Singh, J. Plusquellic, "Defect Detection under Realistic Leakage Models using Multiple IDDQ Measurements", *International Test Conference*, Oct. 2004, pp. 319-328.
31. A. Singh, J. Tharian, J. Plusquellic, "Path Delay Estimation using Power Supply Transient Signals: A Comparative Study using Fourier and Wavelet Analysis", *International Conference on Computer-Aided Design*, Nov. 2003, pp. 748-753.
32. D. Acharyya, J. Plusquellic, "Impedance Profile of Commercial Power Grid and Test System", *International Test Conference*, Oct. 2003, pp. 709-718.
33. J. Plusquellic, D. Phatak, "Localizing Faults in Digital Chips using Steady-State Current Measurements", *NASA Symposium on VLSI Design*, May 2003.
34. A. Singh, D. S Phatak, T. Goff, M. Riggs, J. Plusquellic, C. Patel, "Comparison of Branching CORDIC Implementations", *International Conference on Application Specific Systems, Architectures and Processors*, June 2003, pp. 215-225.
35. C. Patel, E. Staroswiecki, S. Pawar, D. Acharyya, J. Plusquellic, "Diagnosis using Quiescent Signal Analysis on a Commercial Power Grid", *International Symposium on Testing and Failure Analysis*, Nov. 2002, pp. 713-722.
36. S. K. Bahl, J. Plusquellic, J. Thomas, "Comparison of Initial Cell Search Algorithms for W-CDMA Systems Using Cyclic and Comma Free Codes", *Midwest Symposium on Circuits and System Conference*, Volume 3, Aug. 2002, pp. 192-195.
37. A. Singh, J. Plusquellic, A. Gattiker, "Power Supply Transient Signal Analysis Under Real Process and Test Hardware Models", *VLSI Test Symposium*, May 2002, pp. 357-362.
38. C. Patel, F. Muradali, J. Plusquellic, "Power Supply Transient Signal

Integration Circuit", *International Test Conference*, Nov. 2001, pp. 704-712.

39. A. Singh, C. Patel, S. Liao, J. Plusquellic, A. Gattiker, "Detecting Delay Faults using Power Supply Transient Signal Analysis", *International Test Conference*, Nov. 2001, pp. 395-404.
40. C. Patel, J. Plusquellic, "A Process and Technology-Tolerant IDDQ Method for IC Diagnosis", *VLSI Test Symposium*, May 2001, pp. 145-150.
41. J. Plusquellic, A. Germida, J. Hudson, E. Staroswiecki, C. Patel, "Predicting Device Performance From Pass/Fail Transient Signal Analysis Data", *International Test Conference*, Oct. 2000, pp. 1070-1079.
42. A. Germida, J. Plusquellic, "Detection of CMOS Defects under Variable Processing Conditions", *VLSI Test Symposium*, May 2000, pp. 195-201.
43. J. Plusquellic, A. Germida, Z. Yan, "8-bit Multiplier Simulation Experiments Investigating the Use of Power Supply Transient Signals for the Detection of CMOS Defects", *International Symposium on Defect and Fault Tolerance in VLSI Systems*, Nov. 1999, pp. 68-76.
44. A. Germida, Z. Yan, J. Plusquellic F. Muradali, "Defect Detection using Power Supply Transient Signal Analysis", *International Test Conference*, Sept. 1999, pp. 67-76.
45. J. Plusquellic, D. M. Chiarulli, S. P. Levitan, "Characterization of CMOS Defects using Transient Signal Analysis", *International Symposium on Defect and Fault Tolerance in VLSI Systems*, Nov. 1998, pp. 93-101.
46. J. Plusquellic, D. M. Chiarulli, S. P. Levitan, "Identification of Defective CMOS Devices using Correlation and Regression Analysis of Frequency Domain Transient Signal Data", *International Test Conference*, Nov. 1997, pp. 40-49.
47. J. Plusquellic, D. M. Chiarulli, S. P. Levitan, "Digital Integrated Circuit Testing using Transient Signal Analysis", *International Test Conference*, Oct. 1996, pp. 481-490.

Conference Papers: Unpublished

48. M. Martin and J. Plusquellic, "An On-Chip High Resolution Measurement Structure for Measuring Path Delays in an Arbiter PUF", submitted to (blind review), 2013.

Workshops

1. C. Lamech and J. Plusquellic, "Measuring Regional Delay Variations Using A Mux-D Scan Based Embedded Test Structure", accepted *Design for Manufacurability and Yield Workshop*, June, 2012.
2. H. Salmani, M. Tehranipoor, J. Plusquellic, "A Layout-aware Approach for Improving Localized Switching to Detect Hardware Trojans in Integrated Circuits", accepted *International Workshop on Information Forensics and Security*, 2010.
3. R. M. Rad, J. Plusquellic, C. Patel , A. Singh, "Verification of Convolution Relation Between Sensitized Path's Gate Transients, Power Grid Impulse

Responses and Power Port Transients", *D3T Workshop*, co-located with ITC, Nov. 2009.

4. J. Plusquellic, K. Agarwal, D. Acharyya, "Characterizing Within-Die Variation from Multiple Supply Port I_{DDQ} Measurements", *Design for Manufacturability and Yield Workshop*, co-located with DAC, June 2009.
5. H. Salmani, M. Tehranipoor, J. Plusquellic, "New Design Strategy for Improving Hardware Trojan Detection and Reducing Trojan Activation Time", *2nd International Workshop on Hardware-Oriented Security and Trust*, co-located with DAC, June 2009.
6. W. Xiaoxiao, M. Tehranipoor, J. Plusquellic, "Detecting Malicious Inclusions in Secure Hardware: Challenges and Solutions", *1st International Workshop on Hardware-Oriented Security and Trust*, co-located with DAC, June 2008, pp. 15-19.
7. R. Rad, J. Plusquellic, M. Tehranipoor, "Sensitivity Analysis to Hardware Trojans using Power Supply Transient Signals", *1st International Workshop on Hardware-Oriented Security and Trust*, June 2008, pp. 3-7.
8. R. Helinski and J. Plusquellic, "Detecting Small Delay Defects using Self-Relative Timing Bounds", *Defect Based Testing Workshop*, Nov. 2007.
9. R. MohammadPourrad, "Temporal Analysis and Spatial Deconvolution of Power Pad Transients Signals for Fault Localization", *Defect Based Testing Workshop*, Nov. 2007.
10. J. Plusquellic, D. Acharyya, A. Singh, M. Tehranipoor and C. Patel, "Multiple Supply Pad IDDQ-based Defect Detection Techniques Applied to Hardware Test Chips", *Defect Based Testing Workshop*, Nov. 2006.
11. J. Lee, N. Ahmed, M. Tehranipoor, V. Jayaram and J. Plusquellic, "A Novel Framework for Functionally Untestable Transition Fault Avoidance during ATPG", *North Atlantic Test Workshop*, May 2006.
12. J. Plusquellic, D. Acharyya, M. Tehranipoor and C. Patel, "Triangulating to a Defect's Physical Coordinates Using Multiple Supply Pad IDDQs: Test Chip Results", *North Atlantic Test Workshop*, May 2006.
13. N. Ahmed, M. Tehranipoor, C. P. Ravikumar, J. Plusquellic, "At-Speed Transition Fault Testing Using Low Speed Testers with Application to Reduced Signal Enable Routing Area", *North Atlantic Test Workshop*, May 2005.
14. D. Acharyya, A. Singh, M. Tehranipoor, C. Patel and J. Plusquellic, "Sensitivity Analysis of Quiescent Signal Analysis for Defect Detection", *Defect Based Testing Workshop*, May 2005, pp. 3-10.
15. D. Acharyya and J. Plusquellic, "Calibrating Power Supply Signal Measurements for Process and Probe Card Variations", *Defect Based Testing Workshop*, April 2004, pp. 23-30.
16. C. Patel, E. Staroswiecki, D. Acharyya, S. Pawar, and J. Plusquellic, "A Current Ratio Model for Defect Diagnosis using Quiescent Signal Analysis", *Defect*

Based Testing Workshop, April 2002.

17. J. Plusquellic, C. Patel, and Y. Ouyang, "Quiescent Signal Analysis for IC Diagnosis", *System Test and Diagnosis Workshop,* Oct. 2000.
18. J. Plusquellic, D. M. Chiarulli, and S. P. Levitan, "An Automated Technique to Identify Defective CMOS Devices based on Linear Regression Analysis of Transient Signal Data", *Workshop on I_{DDQ} Testing*, Nov. 1998, pp. 32-36.

Invited Talks, Seminars and Tutorials

1. "An Embedded Test Structure for Improving Yield Learning, Profiling New Product Introductions, and Implementing Hardware Security Primitives", Invited talk, *Intel FSM College of Engineering, Technical Seminar Series,* March 2013.
2. "Physical Unclonable Functions and Embedded Test Structures for Hardware-Based Security and Design for Manufacturability", Invited talk, *Arizona State University*, Feb. 2013.
3. "DFT and ATE Working Together to Tackle Next Generation Yield Learning Challenges", Invited talk, *Verigy*, Nov., 2011.
4. "A Truly Embedded Test Structures for Measuring Path Delay Variations in Integrated Circuits", Invited talk, *NVidia*, Nov., 2011.
5. Cyber Security Forum at Sandia, "Power Grid PUF: A Physical Unclonable Function Based on Power Grid Resistance Variations", Invited talk, *Sandia National Laboratories*, Oct. 2011.
6. University Partners, Cyber Open House and Workshop, invitee, Invited talk, *Sandia National Laboratories*, July, 2011.
7. "Power Grid Physical Unclonable Function and Change Detection using Regional Side Channel Analysis", Invited talk, *DARPA*, 2011
8. "Truly Embedded Test Structures for Measuring Power and Delay Variations in Integrated Circuits", Invited talk, *QualComm*, June, 2011.
9. "Minimally Invasive Methods for Characterizing Within-Die Variation", K. Agarwal, D. Acharyya and J. Plusquellic, **INVITED PAPER AND TALK** for Innovative IP Practice session called On-Chip Parametric Sensors, *VLSI Test Symposium*, 2011.
10. "Addressing Process Variability Challenges through better Coupling between Design and Technology", K. Agarwal and J. Plusquellic , **INVITED TALK**, *Design for Reliability and Variability Workshop*, 2011.
11. "Emerging Hardware-Oriented Security and Trust Issues in the Design and Fabrication of Integrated Circuits", **INVITED TALK**, *VLSI Test Symposium*, 2011.
12. "FPGA Applications: From Embedded System Design to Hardware Security and Trust", Invited talk, *Honeywell*, Oct, 2010.
13. "Change Detecting using Regional Power Signal (Side-Channel) Analysis Methods", *Analytical Solutions Inc.* and *DARPA*, Sept, 2010.

14. "Leveraging the Power Grid for Applications in Hardware Security and Trust", *ECE Graduate Seminar*, Sept, 2010.
15. "Experimental Analysis of Regional Leakage and Delay Variations", Invited talk, *NVIDIA*, July, 2010.
16. "Hot Topics in Hardware-Oriented Security and Trust", Invited talk, *Sandia National Laboratory*, July, 2010.
17. "How Much Can I Trust the IC and Hardware?", **INVITED TALK**, *NASA/ ESA Conference on Adaptive Hardware and Systems*, June, 2010.
18. "A Non-Destructive IC Change Detection Method", Invited talk, *Analytical Solutions Inc.*, May, 2010.
19. "A Power Grid Physical Unclonable Function", Invited talk, *UNM Science and Technology Center*, May, 2010.
20. "Design for Manufacturability: Embeddable Test Structures for Measuring Process Variations and Assessing DFM Practice", Invited talk, *IBM ARL*, Nov., 2009.
21. "Design for Manufacturability: Embeddable Test Structures for Measuring Process Variations and Assessing DFM Practice", Invited talk, *Univ. of Texas, Austin*, Nov., 2009.
22. "Leveraging the Power Grid for Applications in Hardware Security and Trust", Invited talk, *ARO Workshop*, Aug., 2009.
23. "Hardware Security: Test Constraints and Implications for ATE", Invited talk, Quarterly Research and Innovation Forum, *Verigy*, July, 2009.
24. "Design for Manufacturability: Embeddable Test Structures for Measuring Process Variations and Assessing DFM Practice", Invited talk, *NVIDIA*, July, 2009.
25. "Leveraging the Power Grid for Applications in Hardware Security and Trust", *Faculty Research Colloquium*, Mar. 2009.
26. "Leveraging the Power Grid for Applications in Hardware Security and Trust", *ECE Graduate Seminar*, Jan. 2009.
27. "Leveraging the Power Grid for Applications in Hardware Security and Trust", *Sandia National Laboratory*, Jan. 2009.
28. "Leveraging the Power Grid for Applications in Hardware Security and Trust", *Microelectronics Research and Development Corporation*, Jan. 2009.
29. "PUFs and Trojan Detection for Hardware Security", *Air Force Research Laboratory*, Dec. 2008.
30. "PUFs and Trojan Detection for Hardware Security", *Air Force Research Laboratory*, Nov. 2008.
31. "Physically Unclonable Functions Derived from Power Grid Resistance Variations", *Xilinx*, Nov. 2008.
32. "Trojan Circuit Detection Techniques and Design for Manufacturability", *Faculty Candidate Interview at University of New Mexico*, May, 2008.

33. "Power Supply Testing Methods for Defect Detection and Identification of Malicious Circuit Inclusions", Invited talk, *CSEE Research Review at UMBC*, May 2007.
34. "Challenges and Solutions to Screening Defective Chips in Nanometer Technologies", Invited talk, *QualComm*, Jan. 2007.
35. "A Solution for Continued Use of I_{DDQ} in DSM Technologies", Invited talk, *NVIDIA*, Nov. 2006.
36. "An RC Test Infrastructure for Monitoring BEOL Process Variations", Seminar, *IBM Austin Research Laboratory*, May 2004.
37. "Defect-Based Test for Defect Detection and Localization", Invited talk, *University of Texas at Austin*, March 2004.
38. "Hardware Results Demonstrating Fault Localization Using Power Supply Signal Measurements", Invited talk and paper, *IBM Austin Center for Advanced Studies Conference*, Austin Research Labs, Feb. 2004.
39. "I_{DDX}-based Fault Localization", Invited talk and paper, *IBM Austin Center for Advanced Studies Conference*, Austin Research Labs, Feb. 2003.
40. "A Current Ratio Model for Defect Diagnosis using Quiescent Signal Analysis", Invited talk and paper, *IBM Austin Center for Advanced Studies Conference*, Austin Research Labs, Feb. 2002.
41. "I_{DDX}-based Testing Methods for Defect Detection, Diagnosis and Performance Characterization", Invited seminar, *Case Western Reserve University*, Nov. 2001.
42. "Multiple Power Supply Pad V_{DDT} Testing for Delay Faults", Invited talk and paper, *IBM Austin Center for Advanced Studies Conference*, Austin Research Labs, Feb. 2001.
43. "Static and Dynamic IDD Methods for Testing, Diagnosing and Estimating Performance of Deep Sub-micron Digital Integrated Devices", Invited talk, *Intel's Manufacturing Test Research Symposium*, Aug. 2000.
44. "The Linux Operating System", Invited talk, *Johns Hopkins Applied Physics Laboratory*, July 2000.
45. "Sharing Good Test Ideas", Invited presentation at IBM in Berlington, May 2000.
46. "Computer Architecture", Invited tutorial, *Texas A&M*, June 1999.
47. "VLSI Design", Invited tutorial, *Texas A&M*, April 1999.
48. "Detecting Fabrication Defects in Digital Integrated Circuits Using Transient Signal Analysis," Invited talk, *Design Technology Center at Hewlett-Packard*, Nov. 1998.
49. "Applications of Transient Signal Analysis for CMOS Defect Detection and Failure Analysis," Invited talk, *University of Pittsburgh*, Oct. 1998.
50. "Digital Integrated Circuit Device Testing using Transient Signal Analysis,"

Invited talk, *Laboratory of Physical Sciences*, University of Maryland, College Park, Feb. 1998.

51. "Digital Integrated Circuit Device Testing using Transient Signal Analysis," Invited talk, *DOD*, Oct. 1997.
52. "Time and Frequency Domain Transient Signal Analysis for Defect Detection in CMOS Digital ICs," Invited talk, *Center for Reliable Computing at Stanford University*, Hosted by Professor Edward J. McCluskey, Nov. 1996.
53. "Time and Frequency Domain Transient Signal Analysis for Defect Detection in CMOS Digital ICs," Invited talk, *Design Technology Center at Hewlett-Packard*, Nov. 1996.
54. "Programming in X Windows, from Xlib to Motif," Tutorial, *University of Pittsburgh*, May 1993.
55. "Neural Network Architectures and Algorithms," Tutorial, *University of Pittsburgh*, March 1992.

Patents

Patent, Jan. 2010, "System and Methods for Generating Unclonable Security Keys in Integrated Circuits"

Patent 7,408,372, August 5, 2008, "Method and Apparatus for Measuring Device Mismatches"

Patent 7,043,389, May 9, 2006, "Method and System for Identifying and Locating Defects in an Integrated Circuit"

Service

Professional Service

2012-2013	Registration Chair, International Symposium on Hardware-Oriented Security and Trust (HOST)
2011	NSF panel, SHF
2011	Appointed Associated Editor, Transactions on Computers, Feb. 2011
2010	NSF panel, CNS
2010-2012	Program Committee, ATE Vision 2020
2010	General Chair, International Symposium on Hardware-Oriented Security and Trust (HOST)
2009	Progam Chair, HOST

2008	**Program Chair**, **Publication Chair** and **Finance Chair**, International Workshop on Hardware-Oriented Security and Trust (HOST). Mohammad Tehranipoor and I co-founded this workshop, which is co-located event at the Design Automation Conference (DAC).
2008	Organizer of the Thesis Research Poster Session at VLSI Test Symposium, May 2008.
2008-2009	Steering Committee, Defect and Data Driven Testing Workshop at the International Test Conference
2007-2009	Program Committee, International Conference on Computer-Aided Design (ICCAD)
2007	Vice-Program Chair for Defect-Based Testing Workshop at the International Test Conference
2006	General Chair for Defect-Based Testing Workshop at the International Test Conference
2005-2009	Program Committee, VLSI Test Symposium (VTS)
2005	Program Vice-Chair for Defect-Based Testing Workshop at VLSI Test Symposium
2004	Program Chair for Defect-Based Testing Workshop at VLSI Test Symposium
2003	Program Co-chair for Defect-Based Testing Workshop at VLSI Test Symposium
2002-2011	Program Committee, International Test Conference (ITC)
	NSF panel member (CISE/CCR/DA)
1999-2003	University Booth Coordinator on SIGDA Advisory Board, ACM

Departmental Service

2010-2011	Computer Engineering Program Chair (1.5 years, Aug 2010 through Jan. 2012), Univ. of New Mexico
2010	Faculty Search Committee, Univ. of New Mexico
2009	Undergraduate Program Committee, Univ. of New Mexico
2008	Graduate Program Committee, Univ. of New Mexico
2007	Publicity Committee, Univ. of Maryland, Balt. Co. Redeveloping college and department level websites, to improve the process of recruiting high quality CMPE undergraduate students.
2007	Faculty Search Committee
2004-2007	Graduate Program Director in Computer Engineering

2002-2003	Graduate Program Director in Computer Engineering
2002	Course scheduling committee
1999-Present	Computer Engineering Graduate Committee Co-authored graduate program proposal submitted to the Maryland Higher Educational Commission for approval in 2001.
1997-2004	Computer Engineering Undergraduate Committee Attended ABET workshop in May 1999.
1997-2004	Faculty Search Committee
1997-2003	Comprehensive Exam Writing and Grading
1997-2001	Equipment Committee Ordered equipment and configured our test and measurement laboratory for the CMPE undergraduate and graduate programs. Successfully solicited for donations from Tektronics and Xilinx in the amount of ~$100K.
1997-Present	Graduate Admissions

New Course Development: Undergraduate

ECE 525 Hardware-Oriented Security and Trust, Fall 2009: The lectures, labs, tutorials, and other course materials are available on webpage (http://www.ece.unm.edu/~jimp/HOST/index.html).

ECE 595 VLSI Synthesis, Fall 2010: The lectures, labs, tutorials, and other course materials are available on webpage (http://www.ece.unm.edu/vlsi_synthesis/index.html).

ECE 443 Hardware Design with VHDL, Fall 2008: The lectures, labs, tutorials, and other course materials are available on wiki page (http://vhdl_fpgas.ece.unm.edu). Videos of the lectures are also available there. Cource material also available on webpage (http://www.ece.unm.edu/~jimp/vhdl_fpgas/index.html).

CMPE 415 Programmable Logic Devices

CMPE 310 Systems Design and Programming

CMPE 413 Principles of VLSI Design

CMPE 414, VLSI Design II

New Course Development: Graduate

ECE 525 Hardware-Oriented Security and Trust, Fall 2009

ECE 522 Hardware Software Co-Design with FPGAs, Spring 2009

CMPE 650 Digital Systems Design

CMPE 646 VLSI Design Verification and Testing

CMPE 640 Advanced VLSI Design

CMPE 641 Topics in VLSI

I applied for MOSIS chip fabrication money for the VLSI design courses over the period from 1998-2002 and supervised student testing of fabricated devices. In 2011, we built a 2 mm X 2 mm chip under a MOSIS research contract in IBM's 90 nm technology. In 2012, we built another 2 mm X 2 mm chip in IBM's 130 nm technology.

Conference and Journal Referee

HOST, ITC, VTS, ICCAD, DAC, Trans. on Circuits and Systems, Trans. on Computer-Aided Design, Trans. on Design Automation of Electronic Systems, NATW, DBT, JETTA, Transactions on Instrumentation and Measurement, Transactions on Information Security and Forensics

Memberships

- IEEE, 1995-Present
- ACM, 1997-2003
- Test Technology Technical Committee (TTTC), 1997-Present