

Memory Types

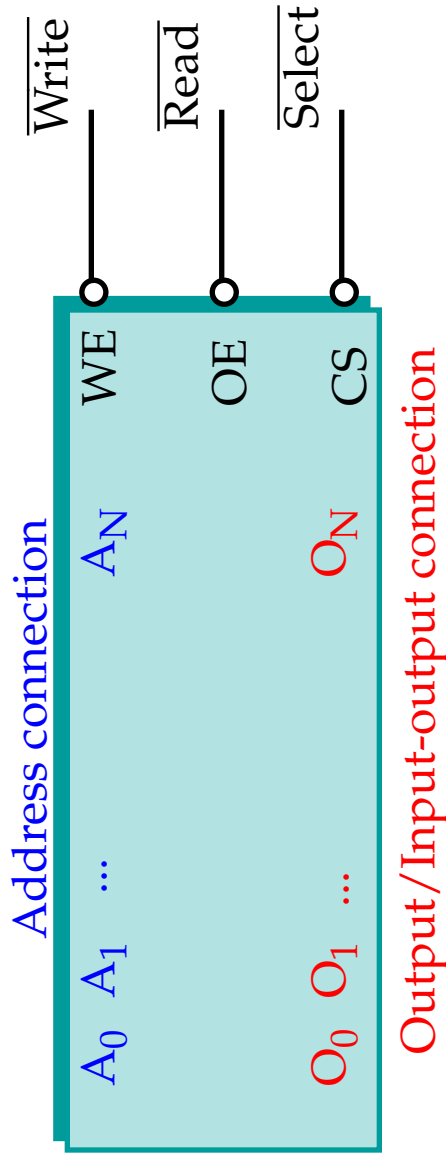
Two basic types:

- **ROM:** Read-only memory
- **RAM:** Read-Write memory

Four commonly used memories:

- ROM
- Flash (EEPROM)
- Static RAM (SRAM)
- Dynamic RAM (DRAM)

Generic pin configuration:



Memory Chips

The number of address pins is related to the number of *memory locations*.

Common sizes today are **1K** to **256M** locations.

Therefore, between 10 and 28 address pins are present.

The data pins are typically *bi-directional* in read-write memories.

The number of data pins is related to the size of the *memory location*.

For example, an 8-bit wide (byte-wide) memory device has **8** data pins.

Catalog listing of *1K X 8* indicate a byte addressable 8K memory.

Each memory device has at least one *chip select* (\overline{CS}) or *chip enable* (\overline{CE}) or *select* (\overline{S}) pin that enables the memory device.

This enables read and/or write operations.

If more than one are present, then all must be 0 in order to perform a read or write.

Memory Chips

Each memory device has at least one control pin.

For ROMs, an *output enable* (\overline{OE}) or *gate* (\overline{G}) is present.

The \overline{OE} pin enables and disables a set of tristate buffers.

For RAMs, a *read-write* (R/\overline{W}) or *write enable* (\overline{WE}) and *read enable* (\overline{OE}) are present.

For dual control pin devices, it must be hold true that both are not 0 at the same time.

ROM:

Non-volatile memory: Maintains its state when powered down.

There are several forms:

- **ROM:** Factory programmed, cannot be changed. Older style.
- **PROM:** Programmable Read-Only Memory.
Field programmable but only once. Older style.
- **EPROM:** Erasable Programmable Read-Only Memory.

Reprogramming requires up to 20 minutes of high-intensity UV light exposure.



Memory Chips

ROMs (cont):

- **Flash EEPROM:** Electrically Erasable Programmable ROM.

Also called **EAROM** (Electrically Alterable ROM) and **NOVRAM** (NOn-Volatile RAM).

Writing is much slower than a normal RAM.

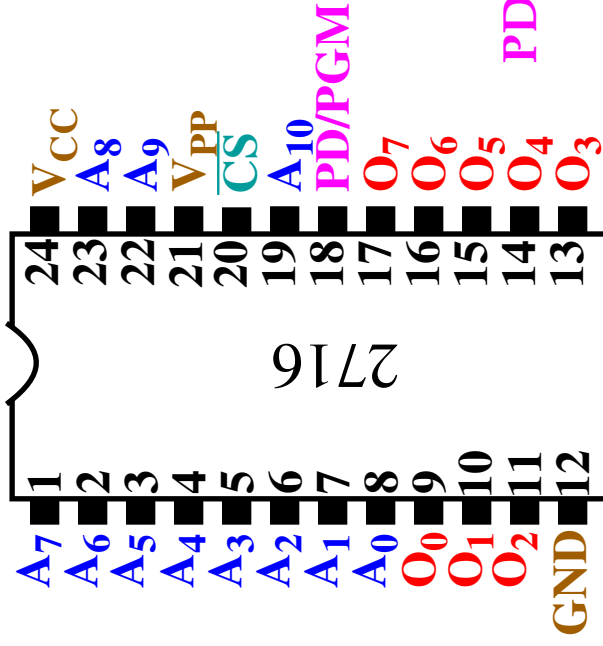
Used to store setup information, e.g. video card, on computer systems.

Can be used to replace EPROM for BIOS memory.



EPROMs

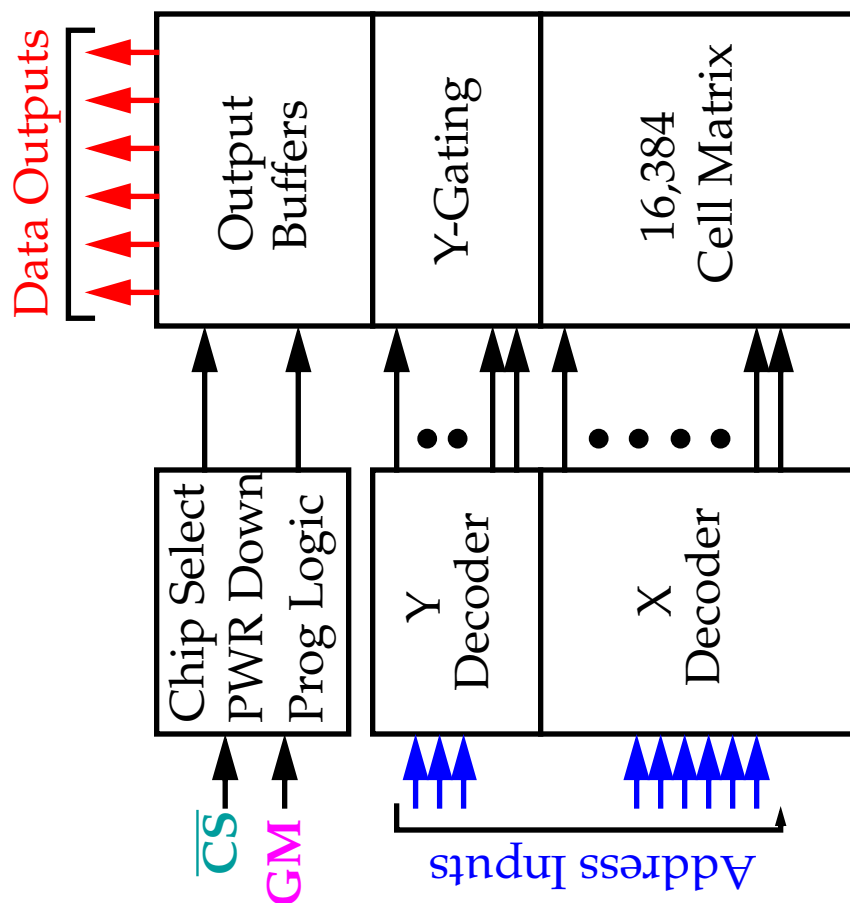
Intel 2716 EPROM (2K X 8):



2K x 8 EPROM

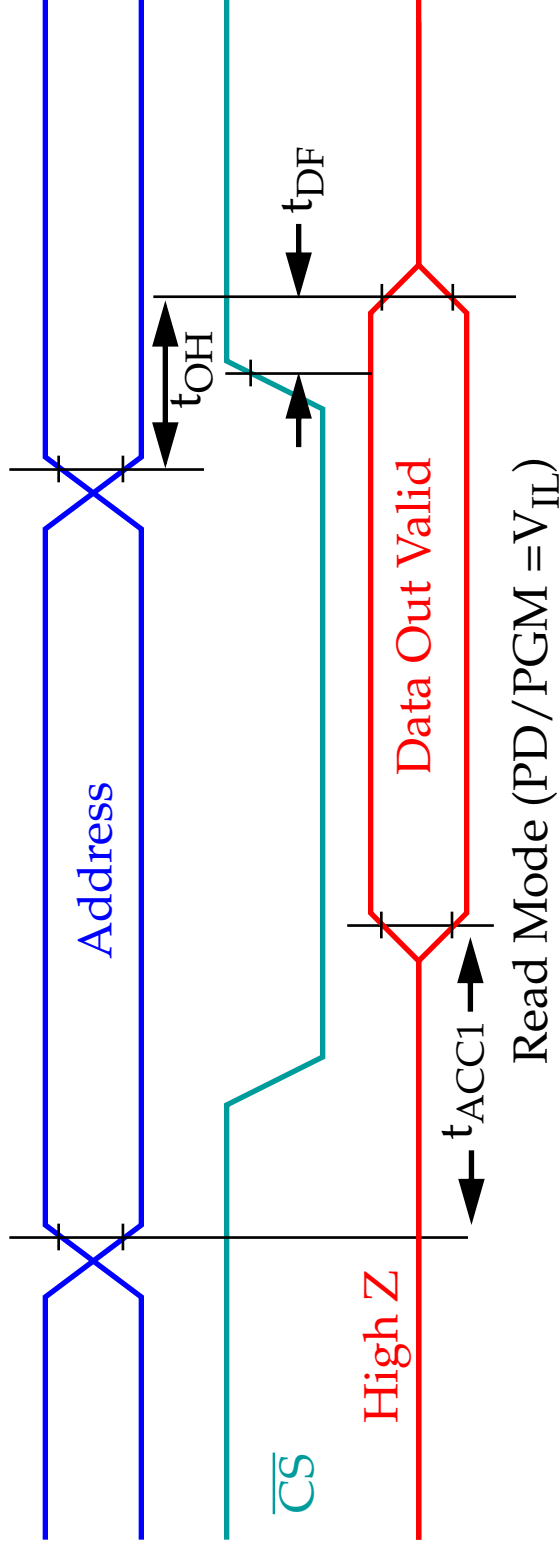
Pin(s)	Function
A0-A10	Address
PD/PGM	Power down/Program
\overline{CS}	Chip Select
O0-O7	Outputs

V_{PP} is used to program the device by applying 25V and pulsing PGM while holding \overline{CS} high.



EPROMs

2716 Timing diagram:



Sample of the data sheet for the 2716 A.C. Characteristics.

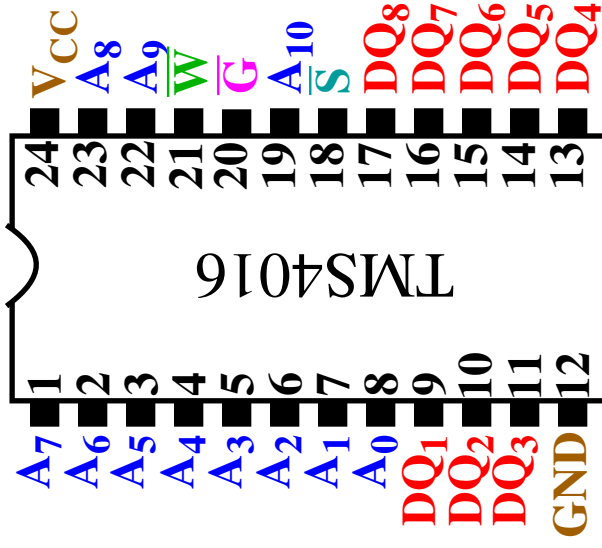
Symbol	Parameter	Limits		Unit	Test Condition	
		Min	Typ.			Max
t_{ACC1}	Addr. to Output Delay		250	450	ns	$PD/PGM = \overline{CS} = V_{IL}$
t_{OH}	Addr. to Output Hold	0			ns	$PD/PGM = CS = V_{IL}$
t_{DF}	Chip Deselect to Output Float	0		100	ns	$PD/PGM = V_{IL}$
...

This EPROM requires a wait state for use with the 8086 (460ns constraint).



SRAMs

TI TMS 4016 SRAM (2K X 8):



2K x 8 SRAM

Pin(s)	Function
A ₀ -A ₁₀	Address
DQ ₀ -DQ ₇	Data In/Data Out
\bar{S} (CS)	Chip Select
\bar{G} (OE)	Read Enable
\bar{W} (WE)	Write Enable

Virtually identical to the EPROM with respect to the pinout.
However, access time is faster (250ns).

See the timing diagrams and data sheets in text.

SRAMs used for *caches* have access times as low as 10ns.



DRAMs

DRAM:

SRAMs are limited in size (up to about 128K X 8).

DRAMs are available in much larger sizes, e.g., 64M X 1.

DRAMs **MUST** be refreshed (rewritten) every **2 to 4 ms**

Since they store their value on an integrated capacitor that loses charge over time.

This refresh is performed by a special circuit in the DRAM which refreshes the entire memory using 256 reads.

Refresh also occurs on a normal read, write or during a special refresh cycle.

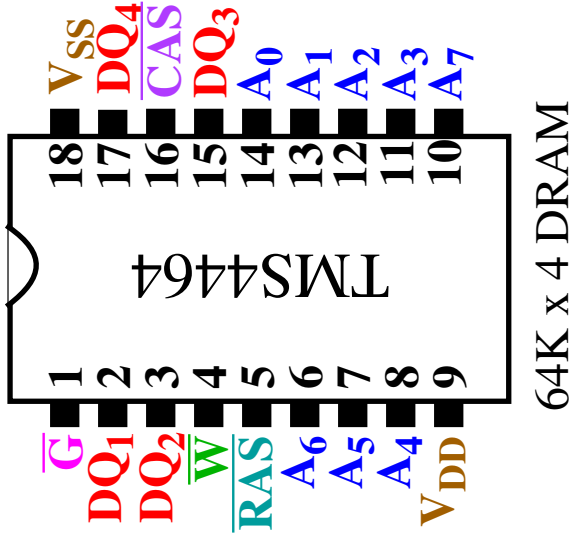
More on this later.

The large storage capacity of DRAMs make it impractical to add the required number of address pins.

Instead, the address pins are *multiplexed*.

DRAMs

TI TMS4464 DRAM (64K X 4):



Pin(s)	Function
A ₀ -A ₇	Address
DQ ₀ -DQ ₄	Data In/Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Write Enable

The TMS4464 can store a total of 256K bits of data.

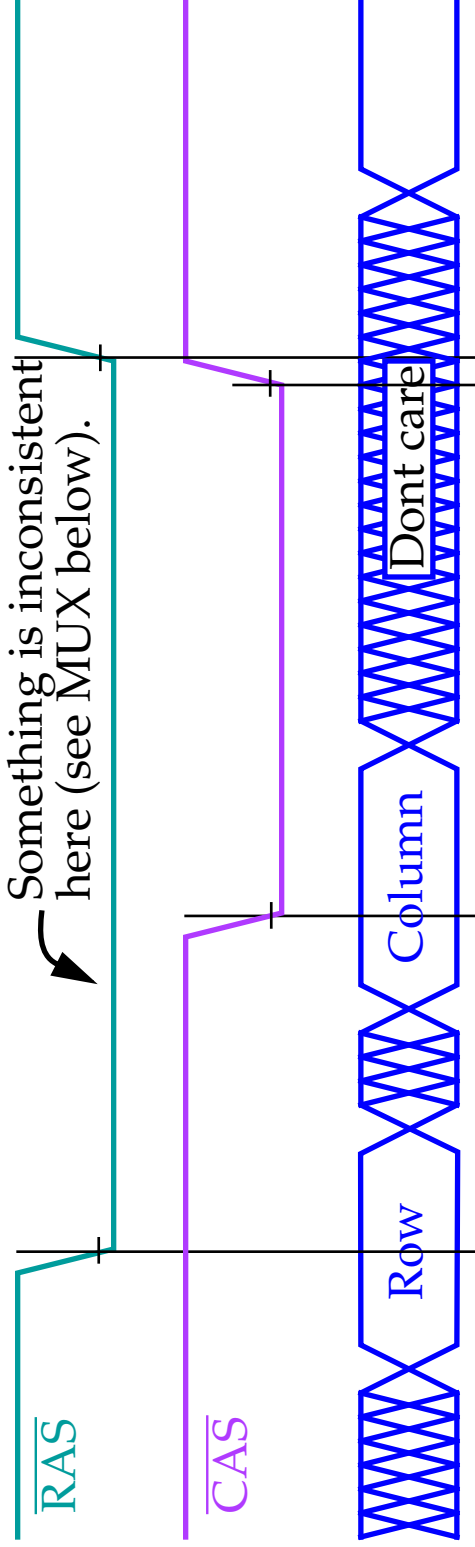
It has **64K** addressable locations which means it needs **16** address inputs, but it has only **8**.

The row address (A₀ through A₇) are placed on the address pins and strobed into a set of internal latches.

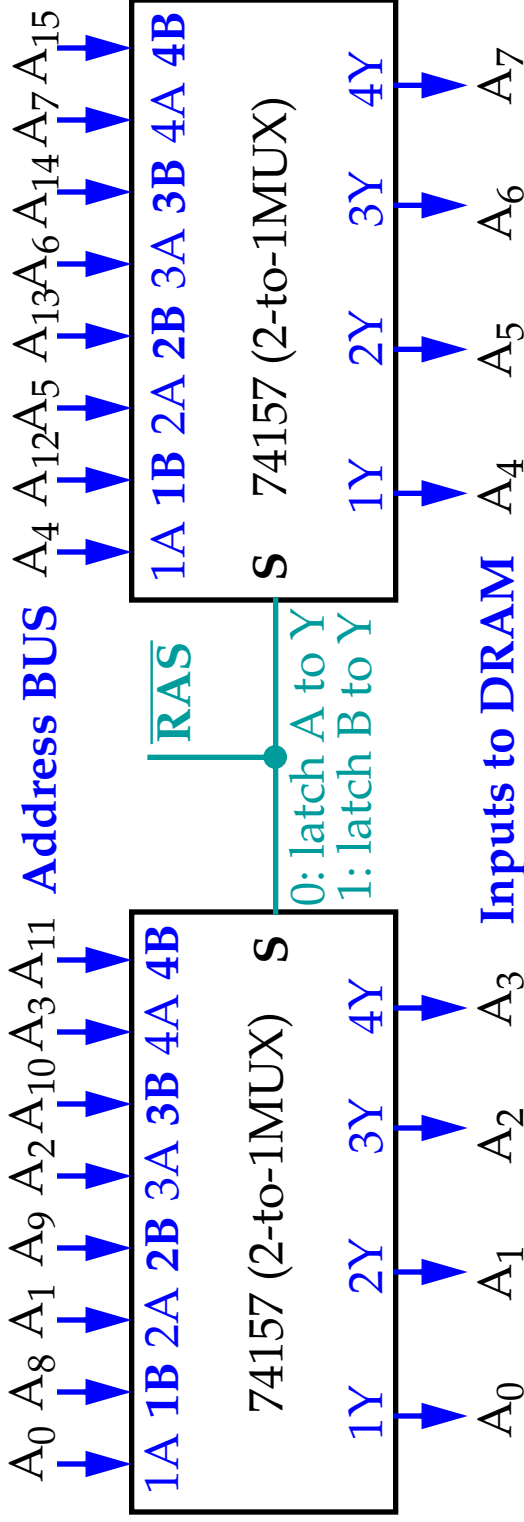
The column address (A₈ through A₁₅) is then strobed in using CAS.

DRAMs

TI TMS4464 DRAM (64K X 4) Timing Diagram:



$\overline{\text{CAS}}$ also performs the function of the chip select input.



Inputs to DRAM



DRAMs

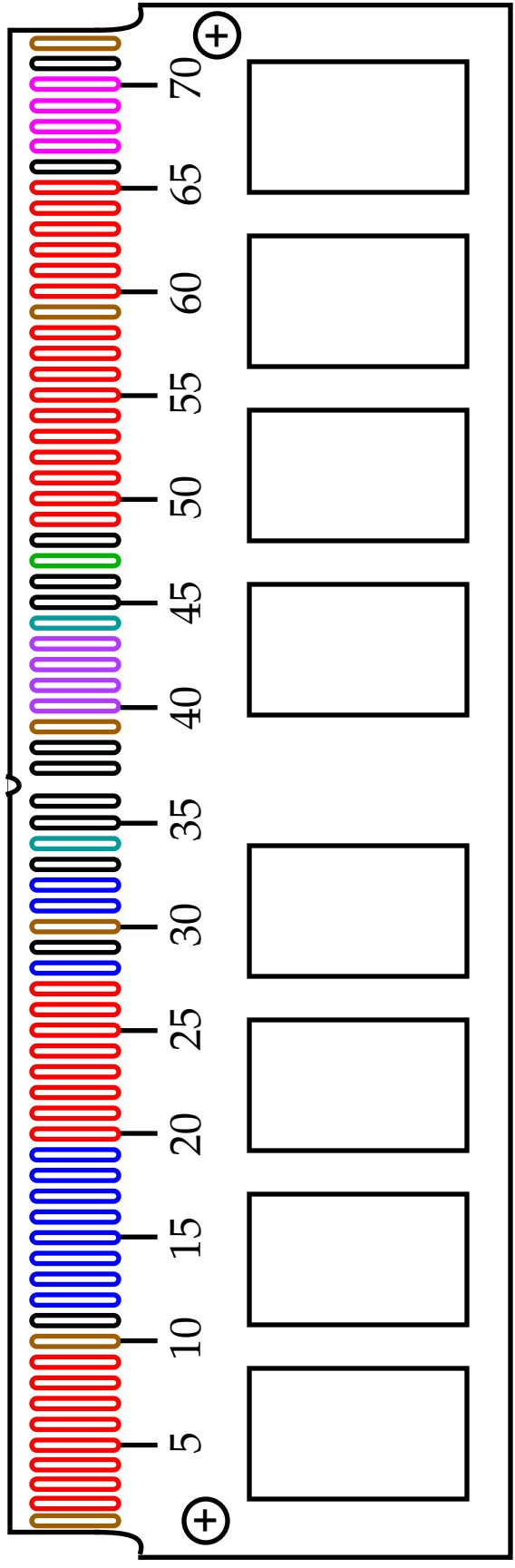
Larger DRAMs are available which are organized as $1M \times 1$, $4M \times 1$, $16M \times 1$, $64M \times 1$ (with $256M \times 1$ available soon).

DRAMs are typically placed on SIMM (Single In-line Memory Modules) boards.

30-pin SIMMs come in $1M \times 8$, $1M \times 9$ (parity), $4M \times 8$, $4M \times 9$.

72-pin SIMMs come in $1/2/3/8/16M \times 32$ or $1M \times 36$ (parity).

V_{SS} **Addr**₀₋₁₁ **RAS** \overline{W} NC
 V_{CC} **DQ**₀₋₃₁ \overline{CAS} \overline{PD}_{1-4}



DRAMs

Pentiums have a 64-bit wide data bus.

The **30-pin** and **72-pin** SIMMs are not used on these systems. Rather, **64-bit DIMMs** (*Dual In-line Memory Modules*) are the standard.

These organize the memory 64-bits wide.

The board has DRAMs mounted on both sides and is **168** pins.

Sizes include **2M X 64 (16M)**, **4M X 64 (32M)**, **8M X 64 (64M)** and **16M X 64 (128M)**.

The DIMM module is available in **DRAM**, **EDO** and **SDRAM** (and **NVRAM**) with and without an EPROM.

The EPROM provides information about the size and speed of the memory device for PNP applications.

