LAB Assignment #1 for ECE 337

Assigned: Mon., Oct. 3, 2011
Due: Mon., Oct. 10, 2011

Description: Learn and understand VHDL-to-hardware synthesis process associated with Conditional Signal Assignment.

This assignment is designed to build your knowledge of combinational logic synthesis using simple signal assignment and conditional signal assignment.

Write the VHDL code for the following arithmetic function (as covered in the lecture)

input ctrl	output result
0 – –	src0 + 1
1 0 0	src0 + src1
1 0 1	src0 - src1
1 1 0	src0 **and** src1
1 1 1	src0 **or** src1

In ISE, create a project, add your VHDL code and 'synthesize' the code. Under the synthesize option, print out the schematic diagrams that are generated. Associate each of the VHDL statements with a specific schematic component that was generated to realize that VHDL statement.

Laboratory Report Requirements:

1) Turn in a commented copy of your VHDL code.
2) Turn in the schematic diagram that represents the synthesized schematic of the code.

Grading:
Correct implementation counts for 70 pts. The remaining 30 pts will be given according to how well the VHDL code is written and documented (comments). Bonus points will be given to any implementation feature that goes above and beyond the requirements.