Midterm Exam

Name:
SSN (last 4 digits):

Total is 100 points.

You must show all of your work -- partial credit may be given to partially correct answers, while answers with no justification may not receive full points. Use the back of the exam sheets if you need extra space.

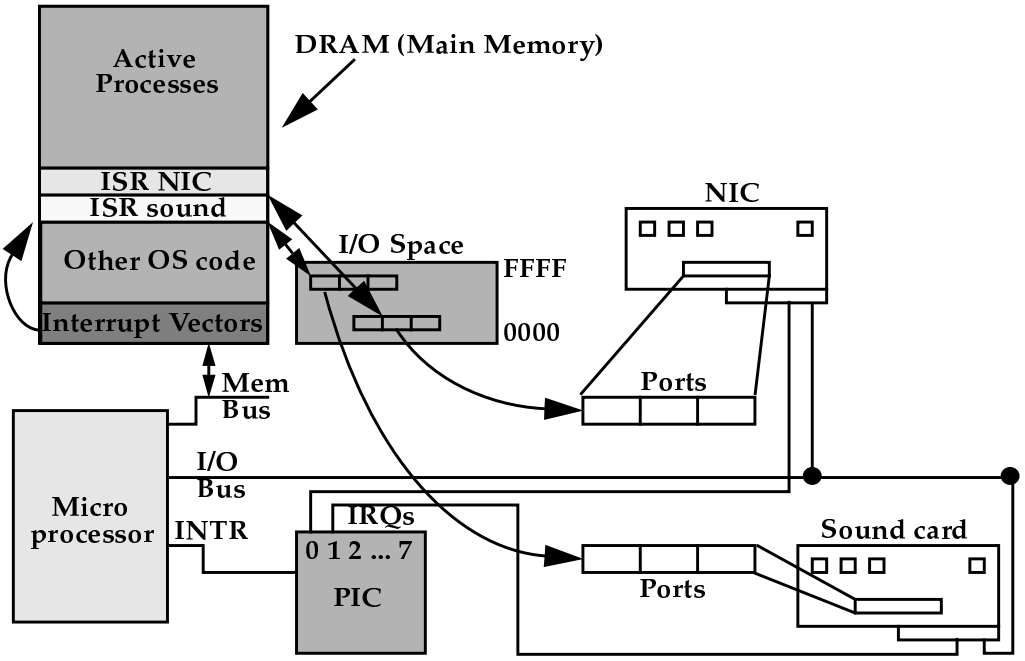
Any instances of cheating or copying found during the exam or during grading will be severely dealt with. You will have to leave the class if found engaging in any form of academic dishonesty during the exam.

This exam is 10 pages long and has 4 questions.

1) a) (3 pts) Give the definition of I/O space as defined under the Intel architecture model? How many I/O devices can be placed in this space assuming each possesses 2 double word registers.

b) (3 pts) Define an interrupt vector? What is the advantage of having interrupt vectors?

c) (6 pts) BRIEFLY explain how an interrupt from the NIC (Network Interface Card) is handled using the following figure.



1) d) (5 pts) What is the difference between external and internal fragmentation?

Which type of fragmentation, if any, will be present in each of the following memory management schemes.
(i) n (possibly unequal) fixed-sized partitions:
(ii) Variable-sized partitions:
(iii) Paging:

e) (8 pts) What is a Translation Lookaside Buffer (TLB)? Explain the steps performed in the translation from a linear to physical address when a TLB is present in the system? What are the advantages of having a TLB?

2) a) (10 pts) What types of addressing modes can be used for each of the following types of functions. List all the modes that apply.

(i) Initialize constants or variables:

(ii) To move a single data value whose address is known:

(iii) To go through each element in an array sequentially where the base and length of the array are known:

(iv) To access single elements in the array where the base of the array is known:

(v) To access a single element in a two-dimensional array where the base is known:

b) (3 pts) What are the elements in a call frame which are setup when you make a procedure call? List them in the order they appear.

c) (2 pts) Define the operation(s) performed by FSUBRP.

2) d) (10 pts) Briefly explain the function performed by the following macro. Explain the answer in terms of the example call shown below.

The macro Something is defined as:

```
%macro Something 3+
        section .data
%1      dd 4
%2      db %3
%%endstr:
        section .txt
        mov dword [%1], %%endstr - %2
%endmacro
```

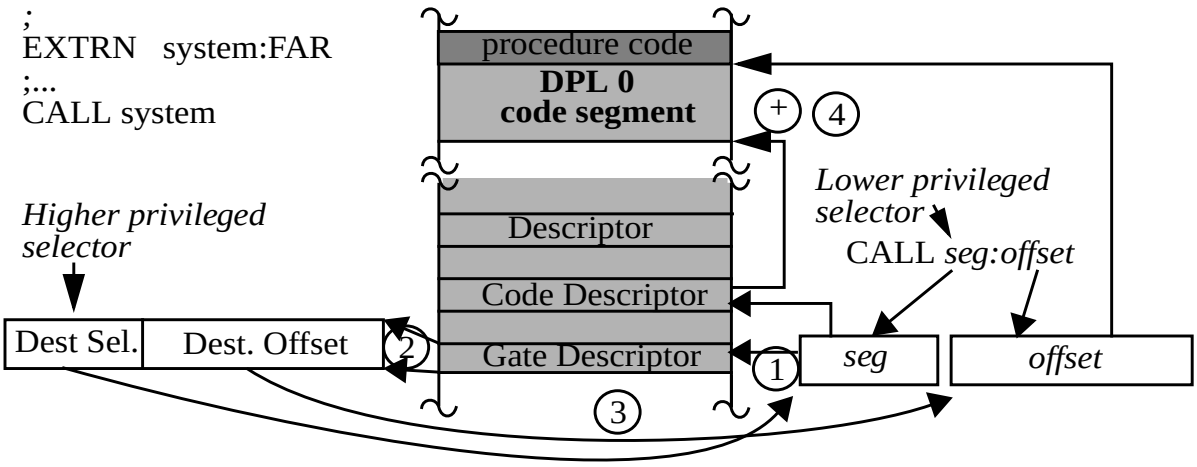
Call to the macro:

Something var1, var2, 'somedata', 0

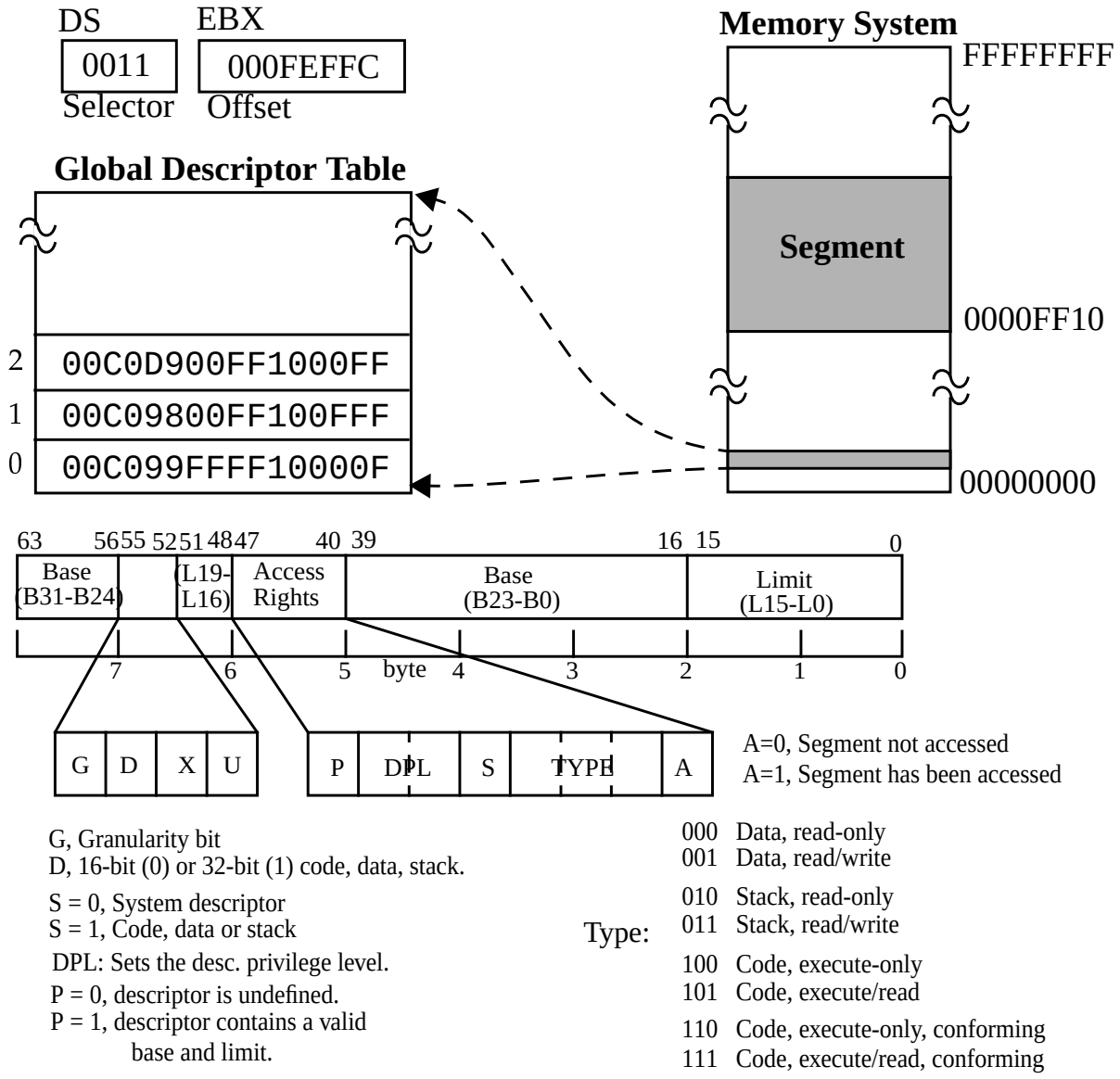
3) a) (4 pts) Briefly explain how the segment registers, e.g. CS, DS, etc. are interpreted in Real mode. Briefly explain how they are interpreted in Protected mode.

b) (4 pts) One purpose of the new segmentation mechanism is to prevent operations on code, data and stacks that do not make sense. Identify two operations that the new segmentation mechanism prevents.

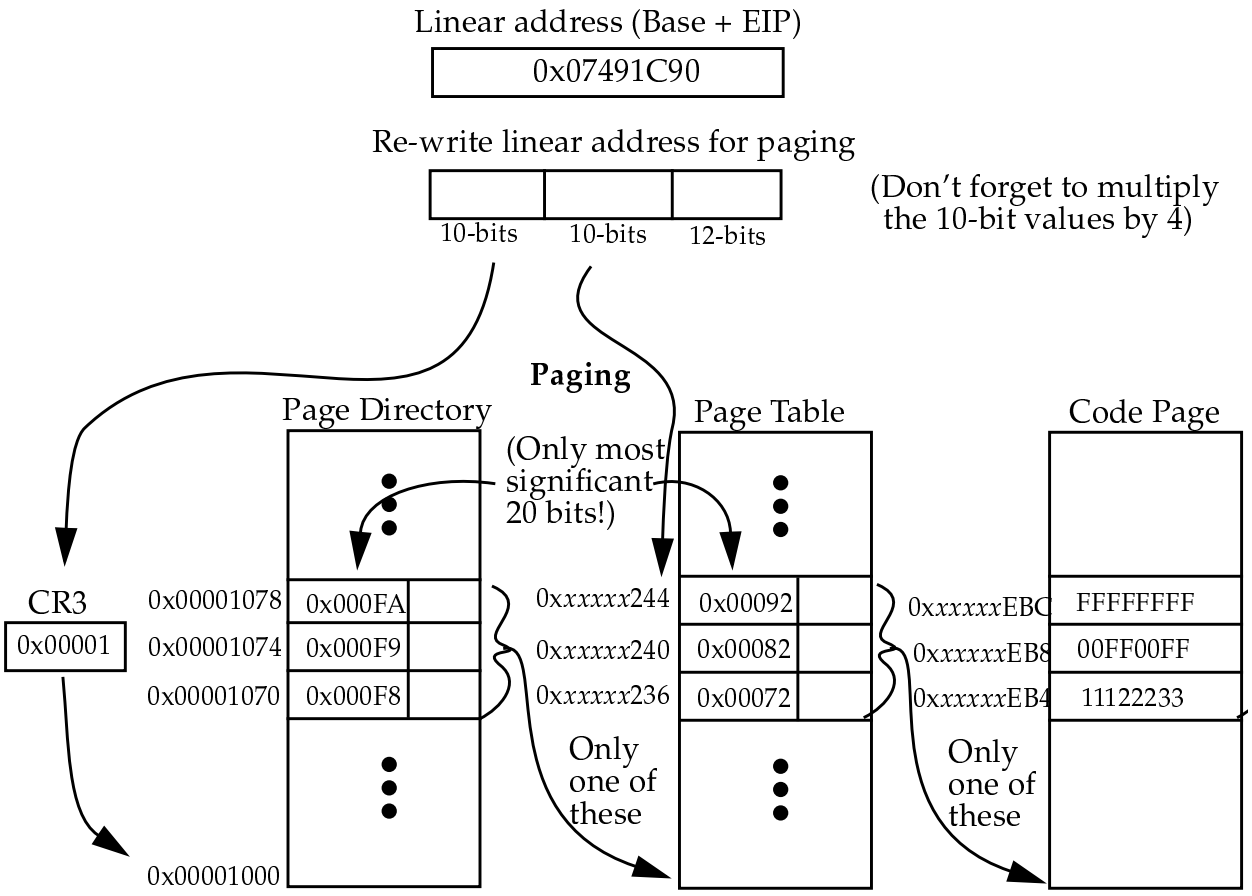
c) (5 pts) Briefly explain in a few words the steps performed as given by 1-4 below. Indicate which step(s) involve privilege checking.



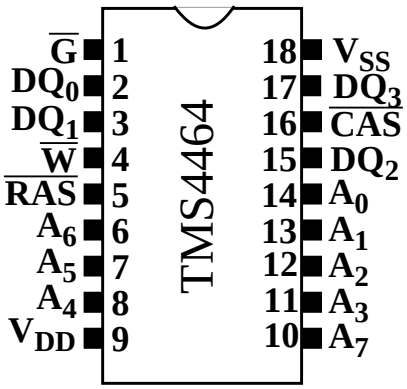
d) (6 pts) Briefly explain the access violations, if any, caused by a process running at privilege level 3 if it issues the follows address as the destination address of a write to memory. Hint: use the descriptor definition to decode the appropriate descriptor.



3) e) (6 pts) Starting with the linear address given, compute the physical address given page table information Be sure to show your work, e.g., give the base addresses of Page Table and Code Page!



4) a) (6 pts) Define and briefly explain the purpose of each of the following sets of pins on the DRAM



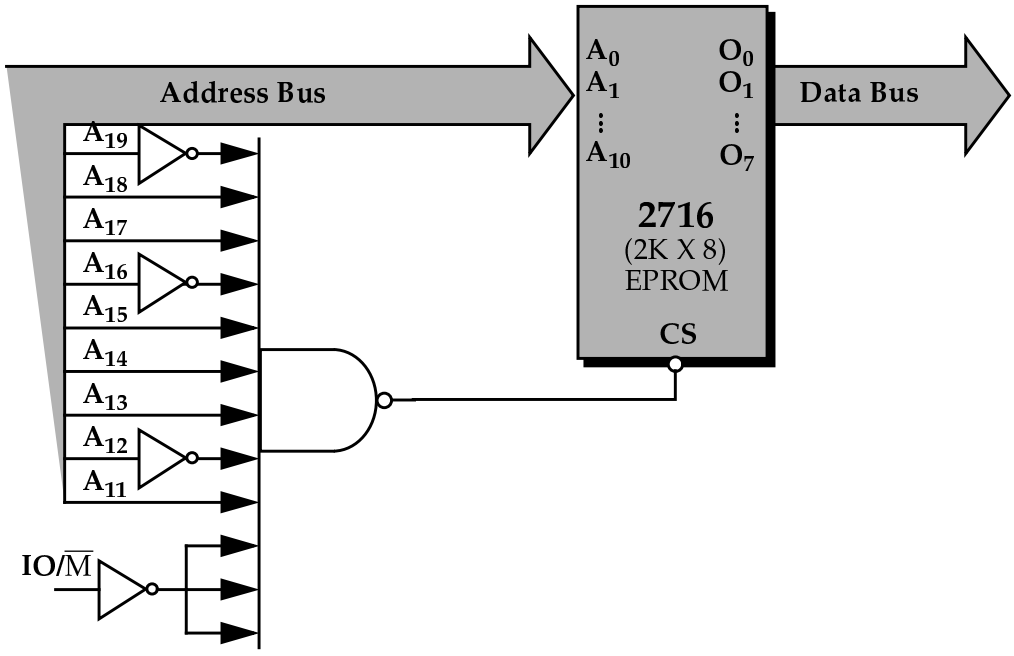
64K x 4 DRAM

i) DQ_0 through DQ_3, A_0 through A_7:

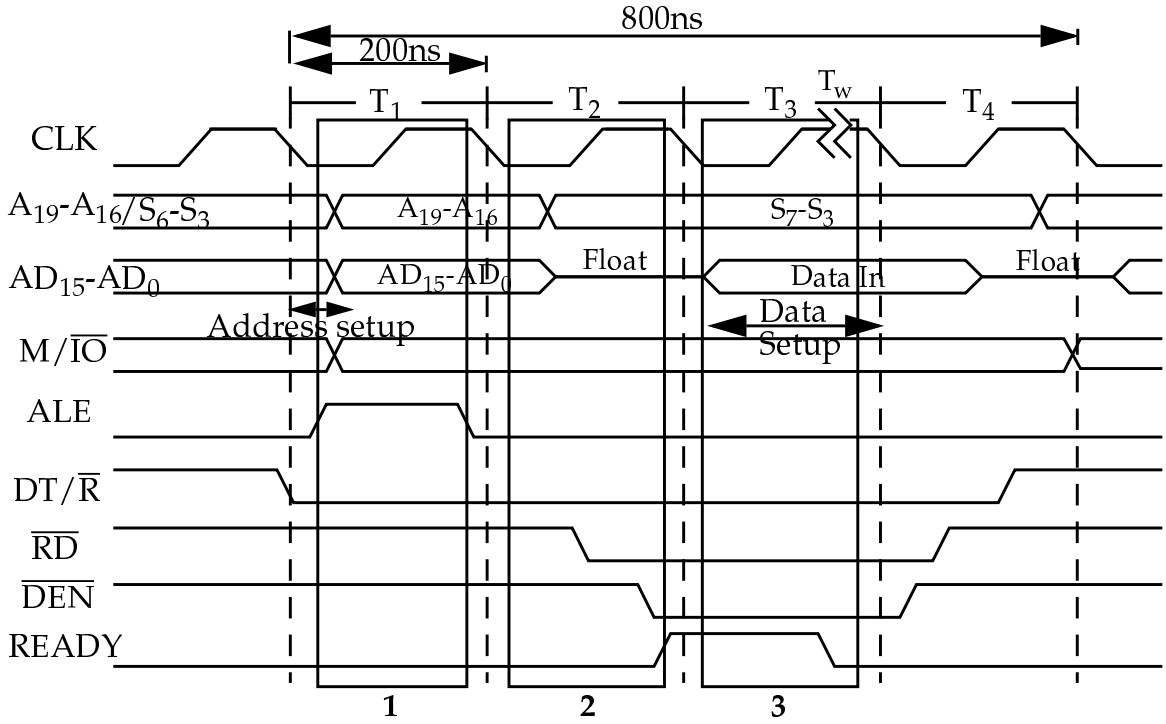
ii) $\overline{CAS}$ and $\overline{RAS}$:

Briefly explain the meaning of the term 64K x 4. What is the size of this memory in bytes?

b) (6 pts) Give the address range in hex that the following memory occupies:



4) c) (6 pts) Briefly explain the operation(s) performed in each of the time periods enclosed in boxes and labeled along the bottom of the following figure. Be sure to indicate whether the operation is being performed by the microprocessor or memory or both. Explain the function of all control signals relevant over the specified time intervals.



Time period **1**:

Time period **2**:

Time period **3**:

d) (3 pts) Name (do NOT explain) three types of erasable non-volatile read/write memories.

e) (4 pts) What does the term Dynamic in DRAMs imply?