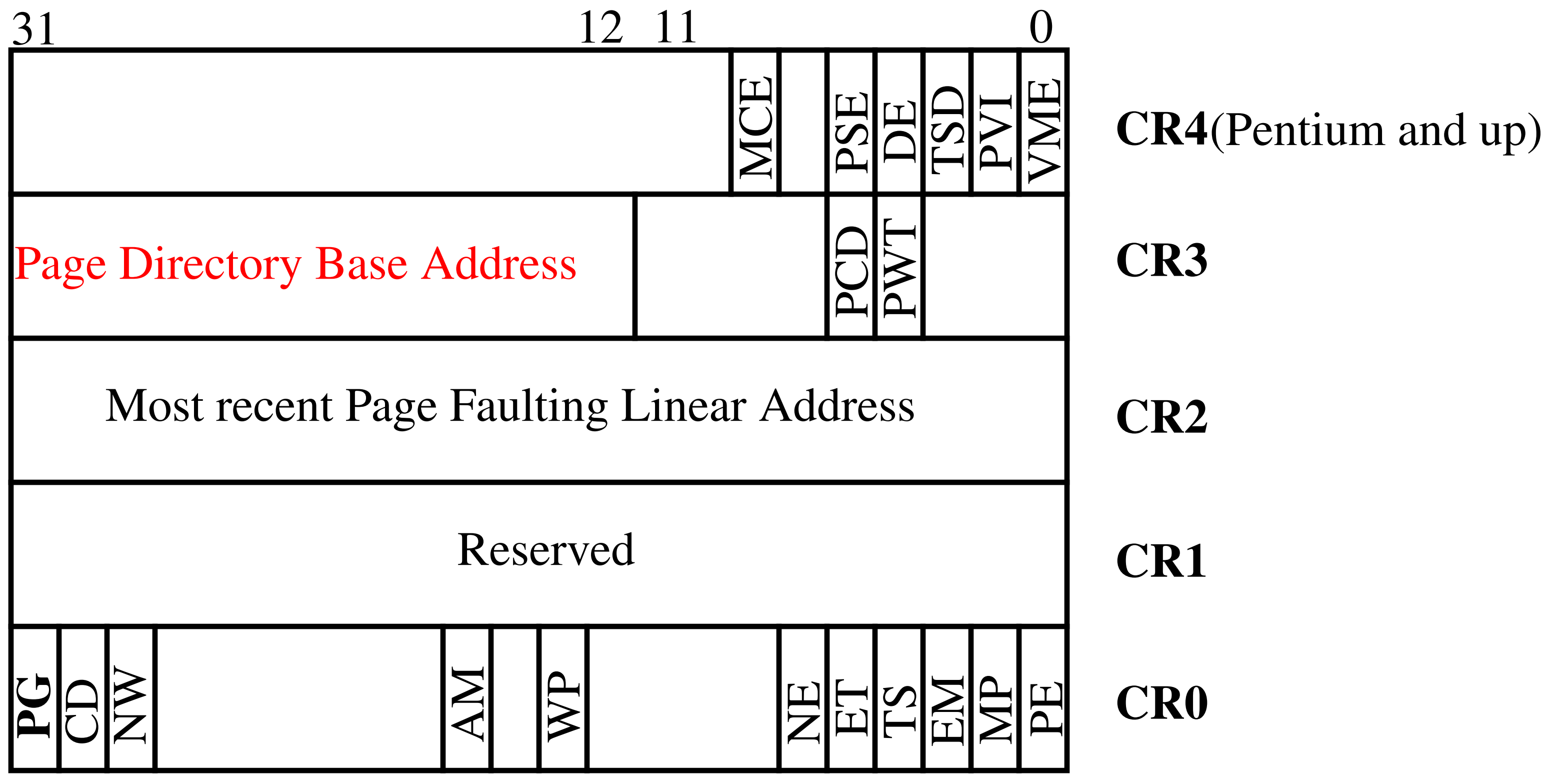
Memory Addressing

Memory Paging:

Available in the 80386 and up.

Allows a *linear address* (*virtual address*) of a program to be located in any portion of *physical* memory.

The **paging unit** is controlled by the microprocessors control registers:



Memory Addressing

Memory Paging:

The paging system operates in both real and protected mode.

It is enabled by setting the **PG** bit to 1 (left most bit in **CR0**).

(If set to 0, linear addresses are physical addresses).

CR3 contains the **page directory** “physical” base address.

The value in this register is one of the few “physical” addresses you will ever refer to in a running system.

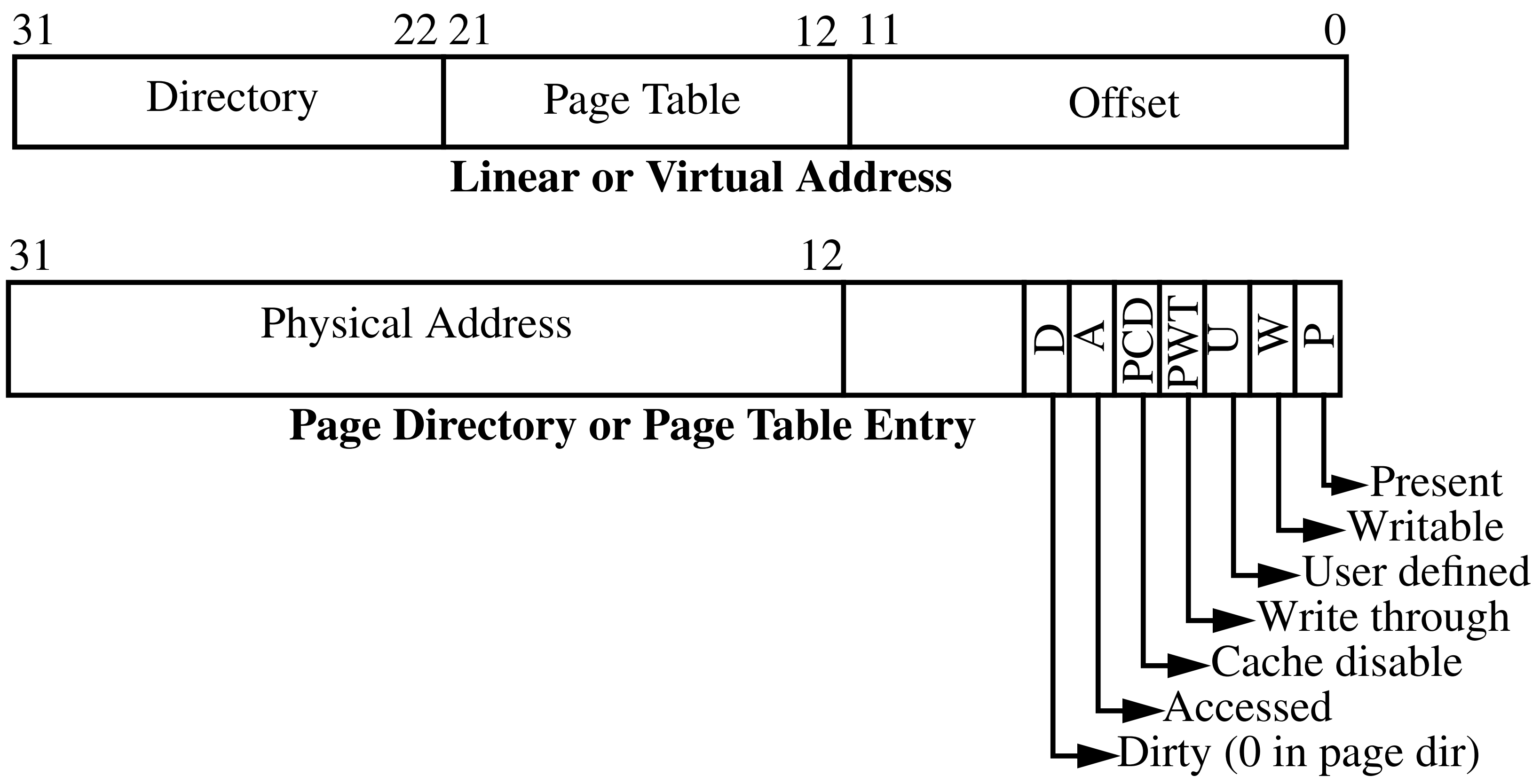
The **page directory** can reside at any 4K boundary since the low order 12 bits of the address are set to zero.

The **page directory** contains 1024 directory entries of 4 bytes each.

Each **page directory** entry addresses a **page table** that contains up to 1024 entries.

Memory Addressing

Memory Paging:

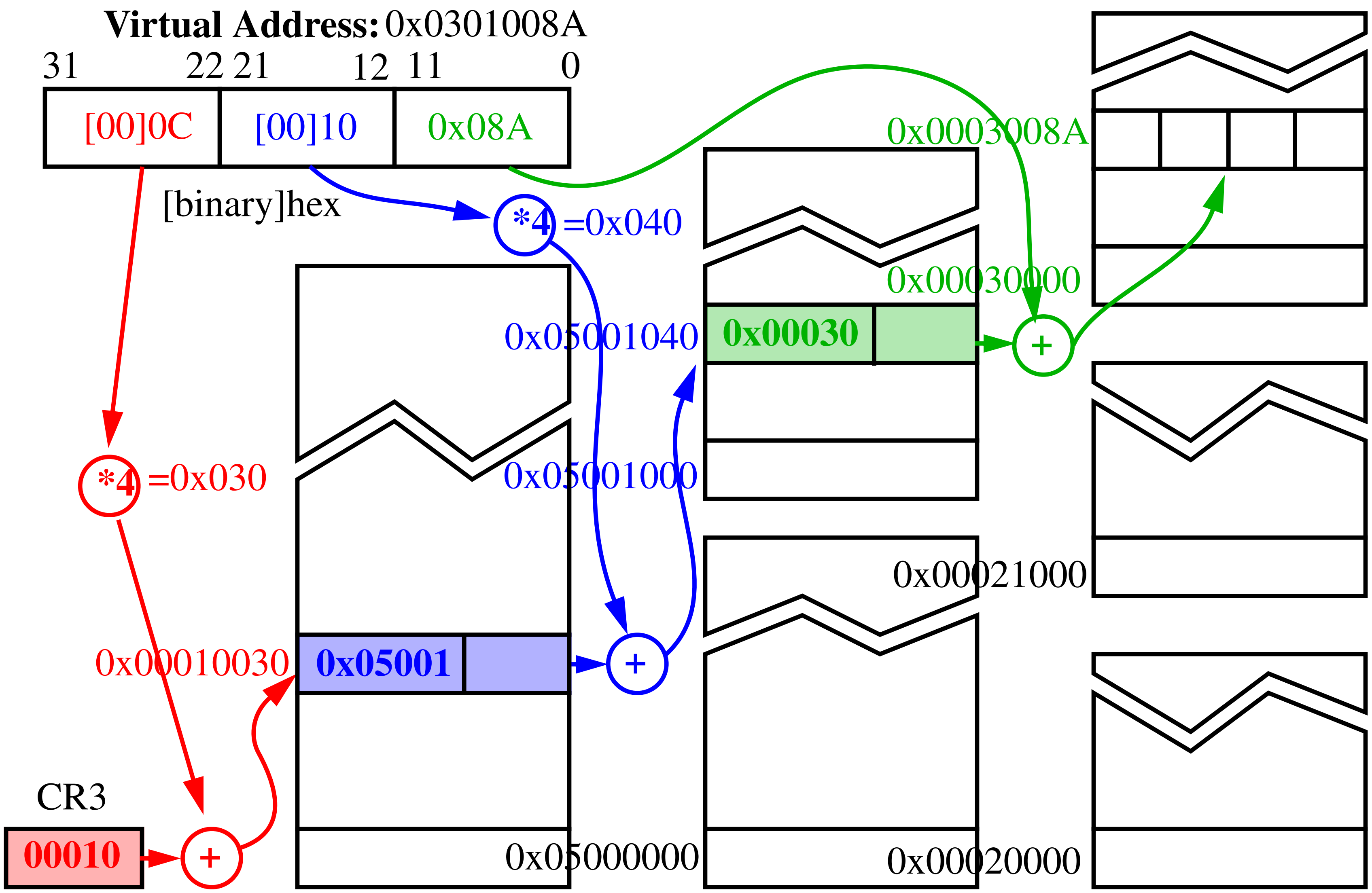


The virtual address is broken into three pieces:

- *Directory*: Each **page directory** addresses a 4MB section of main mem.
- *Page Table*: Each **page table** entry addresses a 4KB section of main mem.
- *Offset*: Specifies the byte in the page.

Memory Addressing

Memory Paging:



Memory Addressing

Memory Paging:

The **page directory** is 4K bytes.

Each **page table** is 4K bytes, and there are 1024 of them.

If all 4GB of memory is paged, the overhead is 4MB!

The current scheme requires three accesses to memory:

One to the **directory**, one to the appropriate **page table** and (finally) one to the desired data or code item. Ouch!

A **Translation Look-aside Buffer** (**TLB**) is used to cache page directory and page table entries to reduce the number of memory references.

Plus the data cache is used to hold recently accessed memory blocks.

System performance would be extremely bad without these features.

Much more on this in OS (CMSC 421).

Paging and Segmentation:

These two addresses translation mechanism are typically combined.

We'll look at this in later chapters.