LAB Assignment #1 for CMPE 415

Assigned: Wed., Sept 20, 2007
Due: Wed., Sept 27, 2007

Description: Modify the verilog code for the led display demonstrated in class to accomplish to the following functions.

The led.v specification uses the 4-bit ‘in’ bus to set the 7-bit ‘out’ bus to one of 15 different values using a case statement. Modify the code to allow the 4-bit ‘in’ bus to implement the following two behaviors:

- If in != 4’b0000, then for each rising clock edge, subtract 1 from a newly declared 24-bit reg variable, count. if count becomes equal to 24’h000000, then increment a newly declared 4-bit ledcnter variable. Use the case stmt to set the state of ‘out’ as we did for led.v.
- if in == 4’b0000, do nothing, i.e., maintain cnter, ledcnter and out in their current states.

You’ll need to add an input parameter, clk, and map it to pin B8 (the 50 MHz clk input to the FPGA). I’ve provided a ucf file ‘led_disp.ucf’ that defines the pin assignments.

Laboratory Report Requirements:

1) Turn in a commented copy of your verilog code.
2) Turn in the schematic diagram that represents the synthesized structural representation of the behavioral code.
3) Run a simulation that shows updates to count, ledcnt and out for changes in the clk and in signals. Print out the waveform window and submit this with your verilog code.
4) Be prepared to demonstrate your code on the FPGA demo boards next Thursday, Sept. 27th.

For this lab, you may work together in groups of three to solve the problem. It is okay, this time, for each member of the group to turn in the same verilog code and schematic. However, I want each of you to run your own simulation experiment. Therefore, I expect to see differences in the waveform printouts that you turn in.

Grading:
60% Verilog code correctly specifies desired functionality.
10% Meaningful comments in verilog code.
30% Meaningful simulation results.