LAB Assignment #2 for CMPE 650

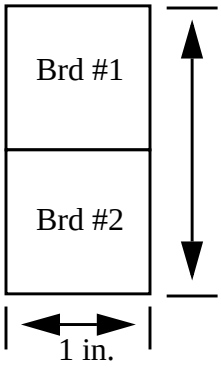
Assigned: Fri., Feb. 22th
Due: Fri., Mar. 7th (layout)
Due: Fri, March 14th (board testing demos)

Description: LAB #2: Test Boards for Measuring Capacitance and Inductance

Part 1: Design two dual sided PCBs (one side as ground plane) using Capture CIS and Layout Plus.

Please refer to Sections 1.6 and 1.7 of your text for details on the board layout. Insert right-angle plastic BNCs (footprint **RF/BNC/R1.350**) on each side of the board. You can use surface mount resistors (footprint **SM/R_1206**) or through-hole resistors for this project. Provide some type of mechanism to allow capacitors to be easily inserted and removed from the test pin locations (footprint **TP**). We can fabricate 10-20 mill wires - proper fabrication below 10 mills is not guaranteed.

Specific instructions:
Design both boards 1 in. X 1 in. with a solid ground plane on the back side. Stack the 1 in. X 1 in. designs vertically:



You MUST use layers TOP and GND for the top and bottom surfaces of the 2-layer board (do NOT use a routing layer and a copper pour). Be sure to set the other layers as ‘unused’ in the layers spreadsheet. Note that Layout Plus shows the GND layer inverted, e.g., black is copper and red is etch (no-copper).

You are allowed to have DRC errors, but only those associated with the BNC posts -- net violations are NOT allowed.

Leave room along the line between the two boards so we can cut them without destroying any of your wiring. Please have your layouts for both boards ready at the beginning at 4pm.

Other suggestions and advice will be posted on my website as it becomes available.

Part 2: Fabricate the boards, solder on the components and carry out a hardware demonstration.

Next friday, we will place each of your layouts into a single layout and we will fabricate the boards. You are responsible for soldering all the components and for performing the experiments as described in the text using discrete capacitors and inductors as test elements.

You will need to purchase the discrete components needed for the boards, e.g., using Digikey or a local electronics shop, e.g., Baynesville Electronics near Towson (http://www.baynesvilleelectronics.com/index2.ivnu)

(I'll try to get the department to buy some of these components, but you should proceed with buying the components for the first lab).

A lab report will be due on March 7th. Describe what you have done and show the results of your measurements and calculations.

Grading:
50% Hardware demonstration successful.
10% Proper board design/components soldered cleanly.
10% Software interface using LABVIEW to collect/display data and perform calculations.
30% Laboratory report description.

NOTES on Capture CIS and Layout Plus: (I'll update this as info becomes available).
Capture CIS:

Layout Plus:
Follow Ekarat's tutorial on creating a new design. Since we are only using two layers and the default technology template has four layers, you'll need to edit the layers spreadsheet, View/Database Spreadsheets.../Layers, right click on the Layer Type field and select Properties, set both BOTTOM and POWER to 'unused (routing)'.

You'll need to move the 'datum' once you've finished the layout but before you've written the GERBER files. It's under Tools/Dimension/Move Datum. We'll need to make sure everyone's design has a different reference point so we can combine them together using ViewMate. Last step is to write the Gerber files, use Auto/Run PostProcessor.