LAB Assignment #3 for CMPE 650

Assigned: Mon., March. 24th
Due: Fri., March 28th (layout)
Due: Fri, April 4th (board testing demos)

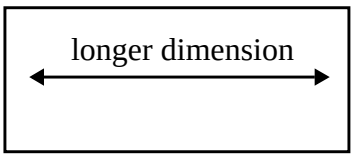
Description: LAB #3: Measuring Metastable States

Part 1: Design a two dual sided PCB (one side as ground plane) using Capture CIS and Layout Plus.

Please refer to Sections 3.11.1 and 3.11.3 of your text for a description of the experiment and details on the board layout (Figure 3.27). You'll need to insert four Molex SMA edge mount connectors (part number 73251-1150: Digi-key: WM5534-ND) on this board for the clk, trigger, data and Q signals, as shown in Figure 3.27. You will also need a potentiometer (BOURNS 3296X), a Hex Inverting Schmitt Trigger (Fairchild semiconductor MM74HC14), a dual D-type positive-edge-triggered FFs w/ clear and preset (Texas Instruments SN74HC74N) -- I will place an order for these parts and update this document if additional information is needed about the footprint. You should use surface mount resistors (footprint **SM/R_1206**) and capacitors. Be sure to make your traces at least 20 mils wide (power wires can be much wider).

The text indicates that the CLR (RESET) input of the FF should be connected with a delayed version of the CLK. You can implement the delay by stringing together two Schmitt triggers, and optionally placing a capacitor between the output of the first and the input to the second to add more delay. I would also recommend that you put a 'jumper' in so that you can disable the automatic reset operation. You'll also want to use a jumper for the switch S_1 given in the book's schematic.

Design the longer dimension of your board horizontally and keep your board real estate as small as possible (see the model board that I have in my office for an example).



You MUST use layers TOP and GND for the top and bottom surfaces of the 2-layer board (do NOT use a routing layer and a copper pour). Be sure to set the other layers as 'unused' in the layers spreadsheet. Note that Layout Plus shows the GND layer inverted, e.g., black is copper and red is etch (no-copper).

You are allowed to have DRC errors, but only those associated with the BNC posts -- net violations are NOT allowed.

We will need to derive new positions for the datums before the laboratory. Please have the layout for your board ready at the beginning of the laboratory (4pm).

Other suggestions and advice will be posted on my website as it becomes available.

Part 2: Fabricate the board, solder on the components and carry out a hardware demonstration.

Next friday, we will place each of your board layers into a single layout and we will fabricate the boards. You are responsible for soldering all the components and for performing the experiments as described in the text.

You will need to purchase the discrete components needed for the boards, e.g., using Digikey or a local electronics shop, e.g., Baynesville Electronics near Towson (http://www.baynesvilleelectronics.com/index2.ivnu). I'll try to get the department to buy some of these components.

A lab report will be due on April 4th. Describe what you have done and show the results of your measurements and calculations.

Grading:
50% Hardware demonstration successful.
10% Proper board design/components soldered cleanly.
10% Software interface using LABVIEW to collect/display data and perform calculations.
30% Laboratory report description.

NOTES on Capture CIS and Layout Plus: (I'll update this as info becomes available).
You'll need to move the 'datum' once you've finished the layout but before you've written the GERBER files. It's under Tools/Dimension/Move Datum. We'll need to make sure everyone's design has a different reference point so we can combine them together using ViewMate. Last step is to write the Gerber files, use Auto/Run PostProcessor.

To force thermal reliefs:
Tools->Footprint->Force Thermal relief (for all nets or one net at time).
To set size:
Options->Thermal Relief Settings (and make sure you spoke width is at least 10)