Final Exam CMPE 650

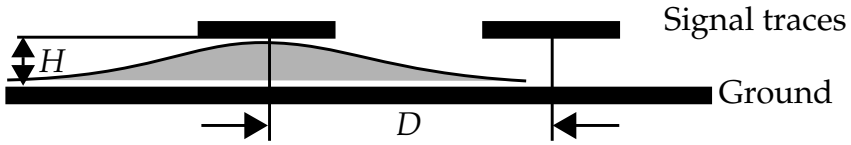
Name:

This exam has 20 questions

You must show all of your work -- partial credit may be given to partially correct answers, while answers with no justification may not receive full points. Use the back of the exam sheets if you need extra space.

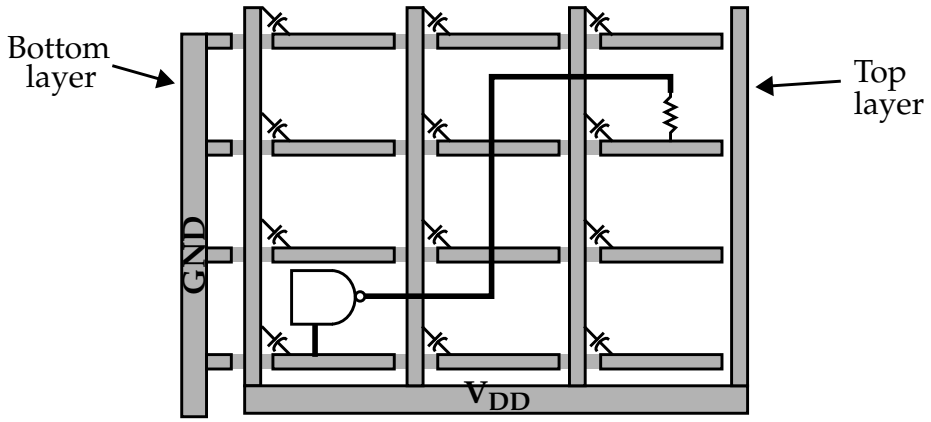
WARNING: KEEP YOUR EYES ON YOUR OWN PAPER. CHEATING OF ANY SORT WILL CAUSE YOU TO FAIL THIS COURSE.

1) (5 pts) The following diagram illustrates current density of the return current under a signal trace. The inductive crosstalk on the neighboring signal trace (on the right) is given by the formula in the figure. Based on your knowledge of inductive crosstalk, what must the variable K depend on?

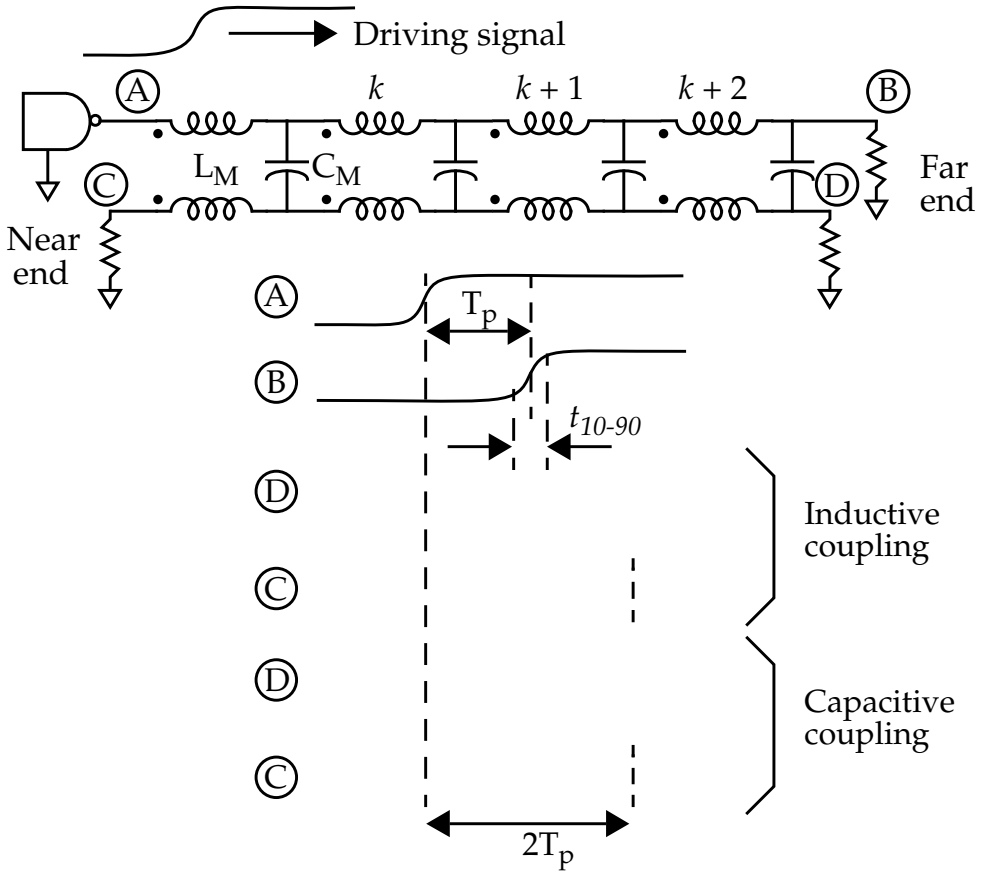


Ratio of measured noise voltage and driving step size $\longrightarrow$ $\text{Crosstalk} = \dfrac{K}{1 + (D/H)^2}$

2) (5 pts) In our discussions over power/GND layout design, we indicated that the following scheme could be used in a two layer board, but would not work well for high speed logic. Briefly explain why this is true. Draw the return current path for the driver shown in the figure.



3) (6 pts) We used the following circuit diagram to model *near-end* and *far-end* crosstalk between lines A-B (agressor) and C-D (victim). Draw the wfms produced at points D (far-end) and C (near-end) under inductive and capacitive coupling, respectively. What is the net effect of the two coupling mechanisms at points D and C?

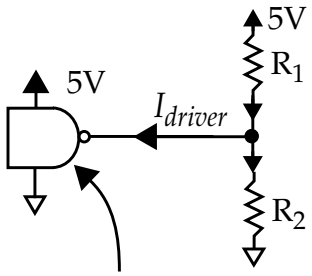


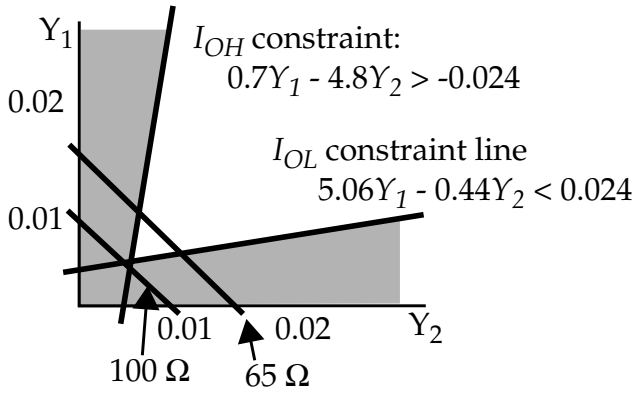
4) (5 pts) With regard to selecting trace width dimensions in board design, most designers do not use the *minimum* width available in the process. Briefly explain the problems associated with using minimum width.

5) (6 pts) Compare/contrast typical configurations of end and series terminations under the following criteria.

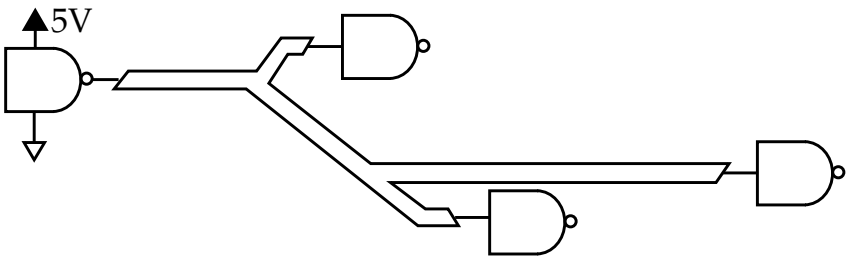
Criteria	End Termination	Series Termination
Propagating voltage amplitude		
Far-end reflection characteristics		
Non-switching state power dissipation		

6) (6 pts) Split termination is proposed as a solution to one of the problems associated with end termination. Proper use of split termination involves several constraints on the values of resistors, R_1 and R_2. Name them and briefly explain how they are denoted in the following constraint graph which uses their corresponding admittances, Y_1 and Y_2.





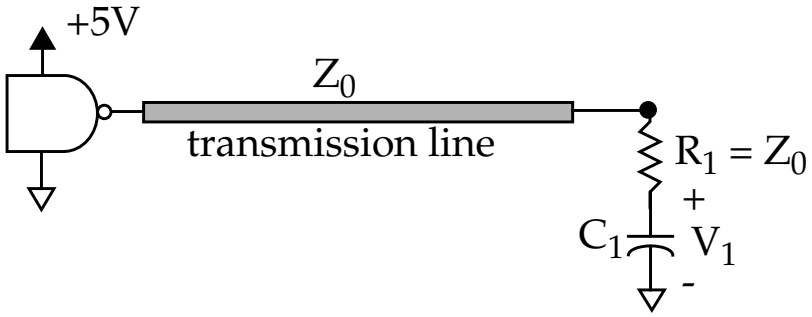
7) (5 pts) What type of termination (end or series) works better for the following circuit topology? Why?



8) (5 pts) Give the constraint on the value of the series termination resistor in series terminated systems.

9) (5 pts) Give the expressions for rise time, $T_{10\text{-}90\%}$, for end and series terminated systems under a capacitive load.

10) (5 pts) Capacitive termination can be used if a certain condition is met (other than the condition that R_1C > system clock cycle time). Name it and give the advantage of capacitive termination over split termination.



11) (5 pts) In order to eliminate reflections in end-terminated systems, the terminating resistor must precisely match the transmission line impedance. Name the sources for mis-match in end-terminated systems.

12) (4 pts) Name the most important property of the power/GND distribution system. Identify two elements of the power supply wiring that reduce this desirable property.

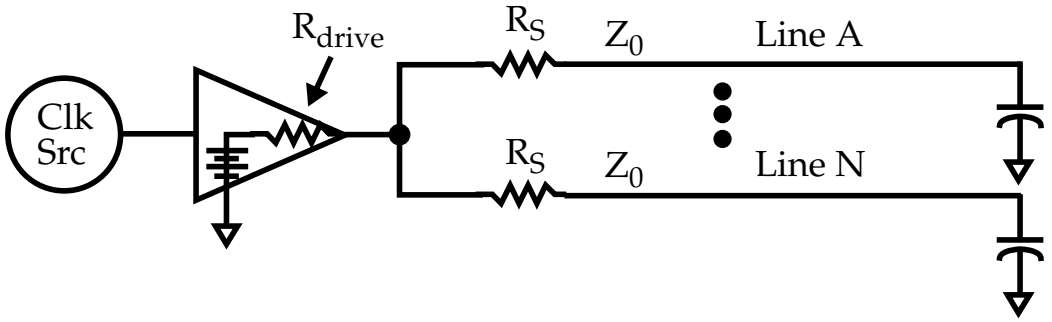
13) (5 pts) By-pass capacitors are used to reduce the *rate-of-change* of current in the power supply wiring. Given the maximum common path impedance, X_{max}, that is tolerable in your system and the inductance of the power supply wiring, L_{PSW}, write the expression that gives the upper bound on the frequency, F_{PSW}, that the power supply wiring alone can support at this impedance.

14) (5 pts) For freqencies above F_{PSW}, a by-pass capacitor is needed. Give the expression for the value of the capacitor designed to keep the power supply impedance below X_{max} for frequencies above F_{PSW}.

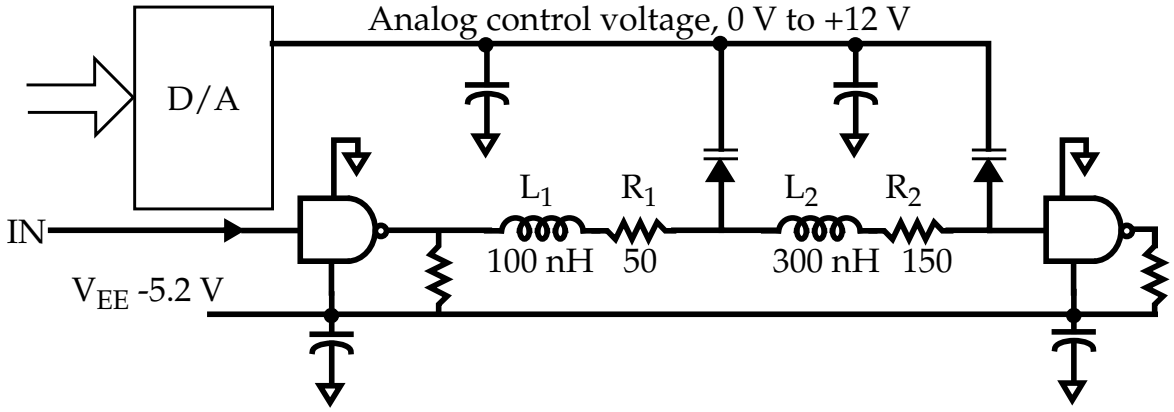
15) (8 pts) By-pass capacitors are only effective up to a certain frequency because of their equivalent series inductance. A second stage of by-pass capacitors, typically an array of capacitors, is used to address this problem. Briefly explain the process (4 steps) of choosing the value for the second stage by-pass capacitors given the constraint that the impedance of the power supply system must be below X_{max} up to frequency F_{knee}.

16) (2 pts) We identified clock skew as a detractor of timing margin in globally synchronous system design. Name two clock distribution topologies designed to minimize skew in systems in which the clock feeds multiple receivers on the board.

17) (4 pts) It is possible to use source termination to distribute the clock, such as that shown below, but under specific conditions. Give the expression for R_S in terms of N, R_{drive} and Z_0.



18) (5 pts) It is sometimes necessary to retard or advance the clock in one part of the circuit with respect to another, for example, as a means of reducing clock skew. Name (do not explain) three ways of adding a *fixed* or *adjustable* delay. Briefly explain how the following circuit allows delay to be adjusted.



19) (4 pts) Name (do not explain) the 4 factors, i.e., allowances, tolerances, etc., that need to be considered in determining the appropriate size of the pad that surrounds a via.

20) (5 pts) How does differential transmission deal with the signal return problem? Realizations of differential systems is never ideal however. Briefly explain this problem as it is illustrated in the following diagram.