Power, Speed and Packages

From VLSI, these look familiar except that *packages* replaces *area*.

Ultimate desire: low power, high speed and cheap packaging.

No logic family satisfies all users.

All logic families offer trade-offs among the three criteria.

Trade-offs:

- Standard packages (those provided by the vendor) saves money but reduces flexibility.

  Standard packages limits both the # of gates and # of pins, which forces systems to be larger, slower, and to use more power for off-chip signals.

- The maximum allowable power dissipation per package is limited by package construction and the cooling system employed.

  As chip density increases, systems get smaller and cheaper to manufacture, but often dissipate more total power, which limits the # of gates.

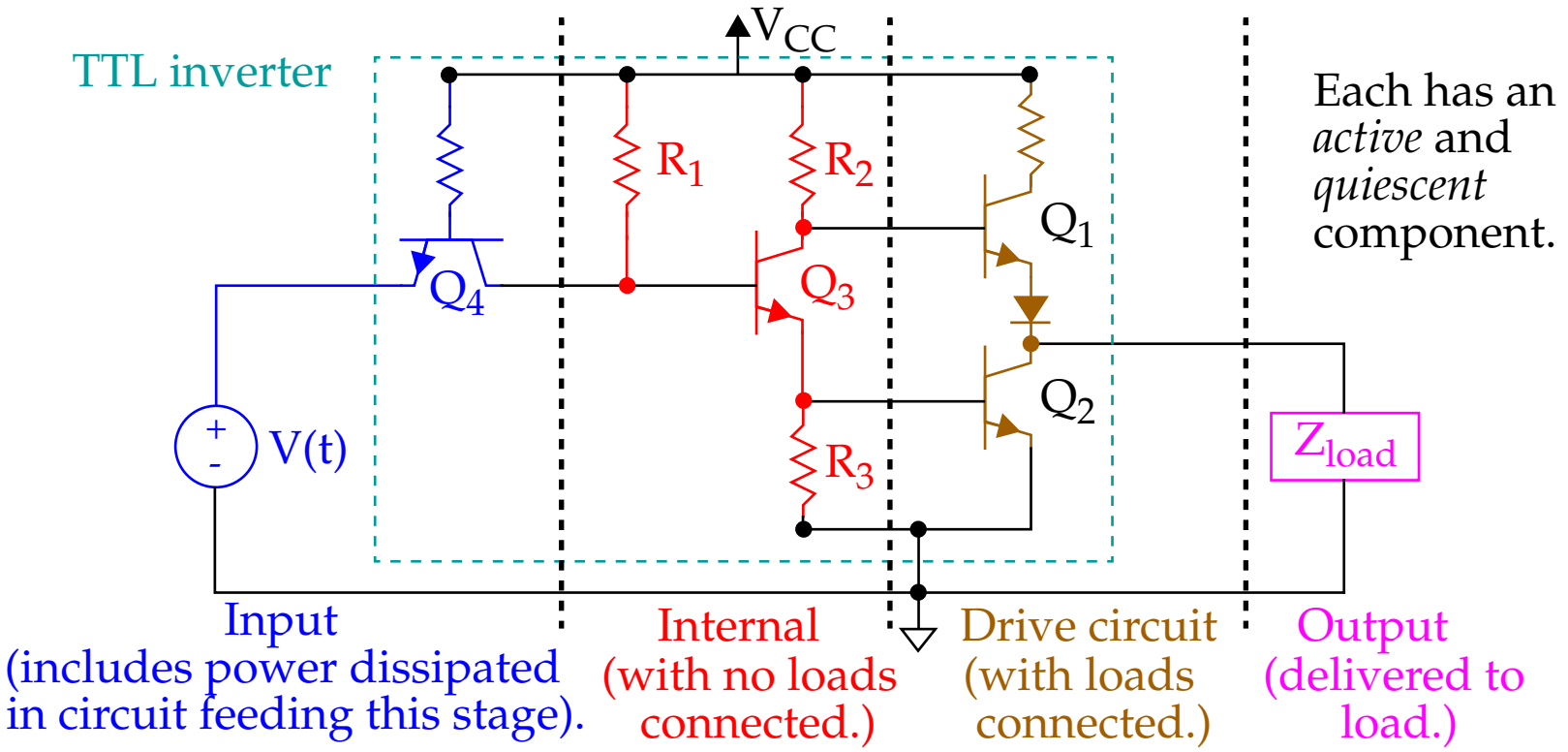
- Higher speed chips usually dissipate more power.

Power

The typical supply current, I_{CC}, on the data sheet is only indirectly related to power dissipation.

Rated I_{CC} often doesn't consider additional power dissipation that occurs at high speed and power used to drive heavy output loads.

Break down of power consumption within a circuit:



Quiescent vs. Active Power Dissipation

Quiescent power maintains the logic state (usually what is quoted in spec.)

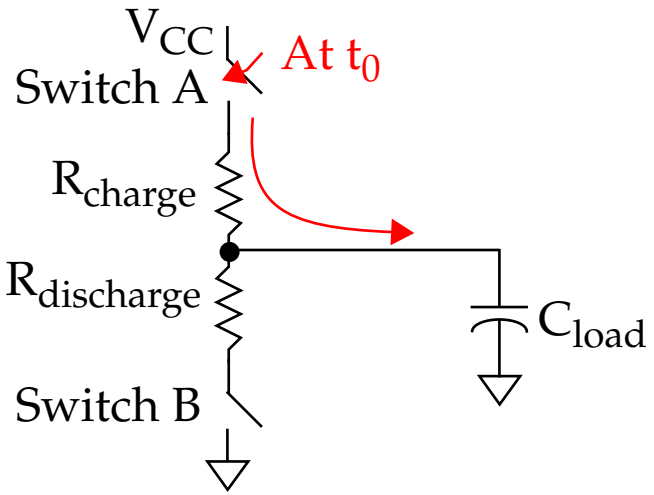
Computed by measuring current *I* and delta *V* across resistors and summing *I*V* components.

Active power is:

$Power$ = (cycle frequency)(additional energy used per cycle beyond quiescent)

Most common sources of **active power dissipation** are **load capacitance** and **overlapping bias currents**.

- We've analyzed power dissipation due to load capacitance in VLSI, i.e.



At time t_1, Switch A closes.
Power dissipated on R_{charge}

At time t_2, Switch B closes.
Equal amount of power dissipated on $R_{discharge}$

Quiescent vs. Active Power Dissipation

The energy per cycle is given by.

$$\text{Energy per cycle} = CV_{CC}^2$$

Add frequency to convert to power:

$$\text{Power} = fCV_{CC}^2 \qquad \text{(valid for CMOS or TTL circuits)}$$

- We ignored the crowbar power dissipation (in VLSI), here called **overlapping bias currents**.

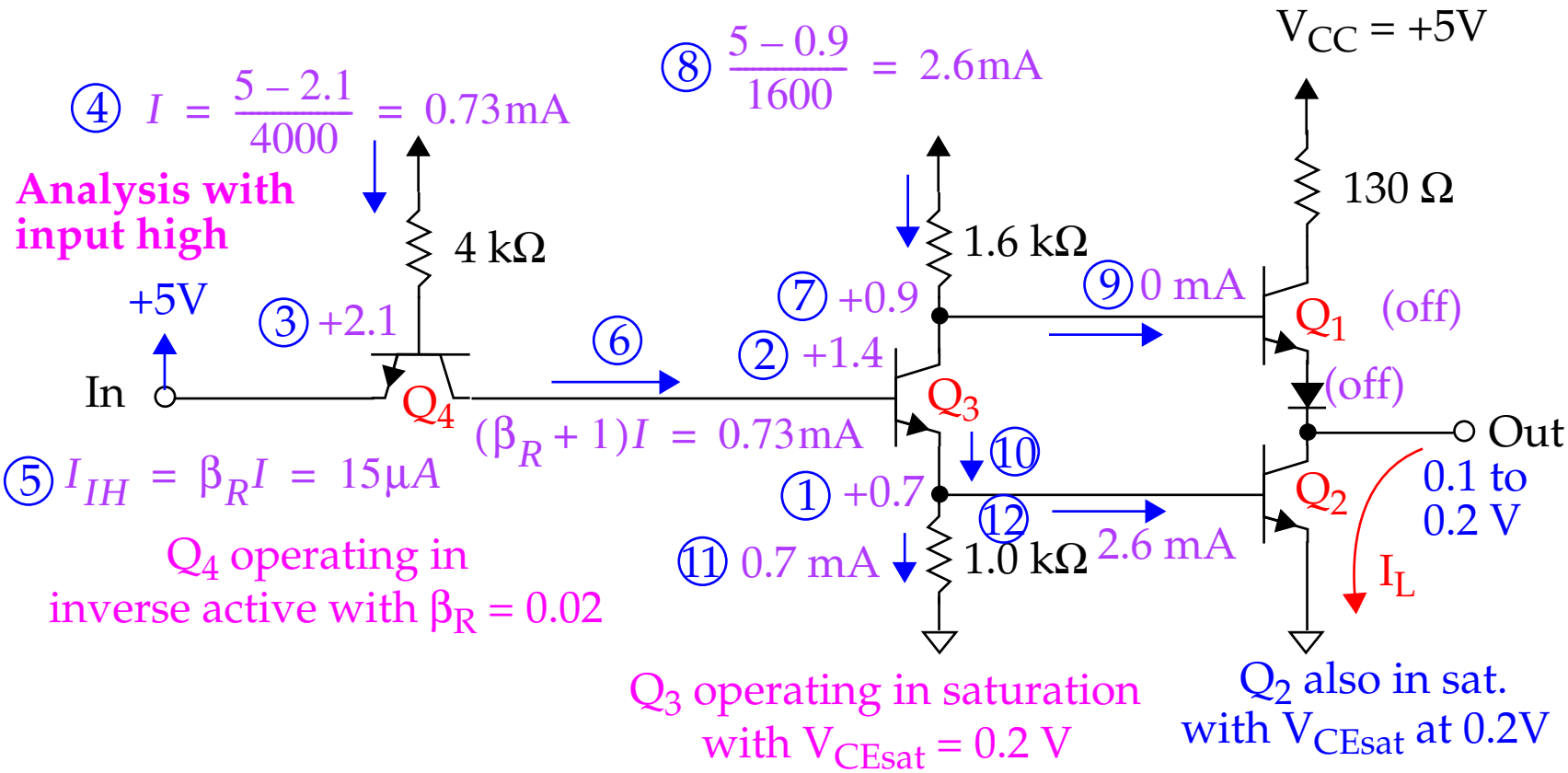
  TTL (and CMOS) have a **totem-pole** output stage where the output is actively driven HI and LO.

  For TTL (see inverter), this occurs by turning on Q_1 or Q_2, but not both.

  Every logic family that uses a totem-pole arrangement has a mechanism that ensures the pull-up and pull-down networks don't conduct simultaneously.

Active Power Dissipation

From the TTL inverter, the diode ensures that Q_1 is completely off when Q_2 and Q_3 fully saturate to pull output LO.



Note that diode is needed since with 0.9 V on base of Q_1 would turn it on. Also, the load current I_L is limited to about 25 mA to keep Q_2 in sat.

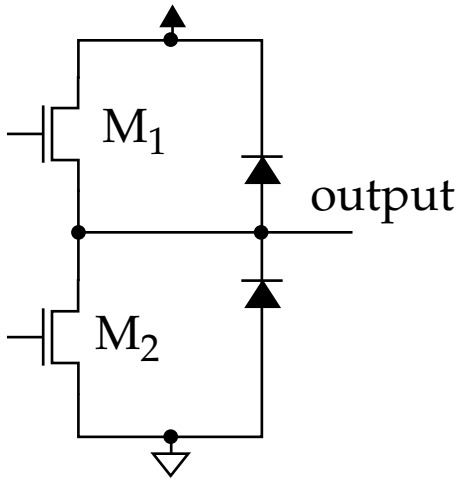
Active Power Dissipation

During switching, Q_1 and Q_2 simultaneously conduct for a short period of time, dissipating power.

This occurs because charge on base of Q_2 is drawn off by 1 kΩ resistor (which takes time) while Q_1 turns on almost immediately.

The 130 Ω resistor in series with Q_1 "protects" by limiting the magnitude of this shorting current.

CMOS circuits can also be constructed as totem-pole, for example,



Input Power

Input power is supplied by the input drivers.

Input parameter	74HCT00(**CMOS**)	74AS00(**TTL**)	10H101(**ECL**)	10G001(**GaAs**)
I_{in} HI (mA)	0	+0.020	+0.425	+0.400
I_{in} LO (mA)	0	-0.500	+0.0005	-0.100
$P_{quiescent}$ (mW)	0	1.3	1.1	1.3
input C (pF)	3.5	3	3	1.5
delta V_{in} (V)	5.0	3.7	1.0	1.5
P_{active} (mW)				
f = 1MHz	0.09	0.04	0.003	0.003
f = 10MHz	0.9	0.4	0.03	0.03
f = 100MHz			0.3	0.3
f = 1000MHz				3.0

Quiescent power is determined by multiplying required input current by supply voltage (gives sum of power dissipated in driver and receiver).

Active power computed using input cap., supply voltage and frequency:

Power = fCV_{CC}^2

Internal Dissipation

Internal power is used to bias and switch nodes internal to a logic device.

Quiescent and active power are measured without loads attached.

Quiescent power is measured for random input states using a current meter in series with the power pin.

Active power is measured for some frequency *f* using:

$$K_{active} = \frac{P_{total} - P_{quiescent}}{f}$$

and then for any frequency:

$$P_{total} = P_{quiescent} + f K_{active}$$

CMOS exhibit a clear linear relationship between internal dissipation and freq because their leakage is small. TTL exhibits linearity at higher freqs.

Because of their smaller voltage swing, ECL and GaAs show little increase in power with frequency (because of V^2 term).

Drive Circuit Dissipation

This is where most of the power is dissipated.

Parameters include:

- Output circuit configuration
- Logic levels
- Output load
- Speed of operation

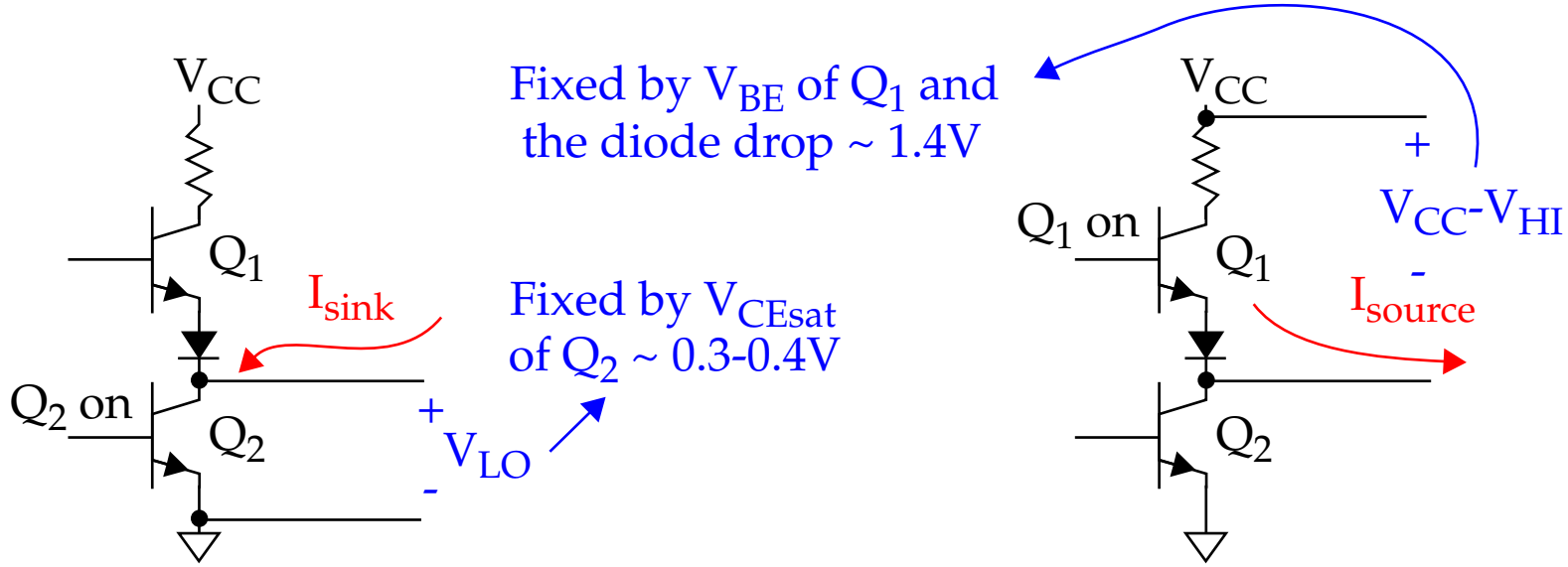
Four popular output configurations:

- Totem pole
- Emitter follower
- Open collector
- Current source

The details of the output driver characteristics are important to understand when we later look at transmission lines.

Drive Circuit Dissipation

Quiescent power in TTL **totem-pole** configuration:



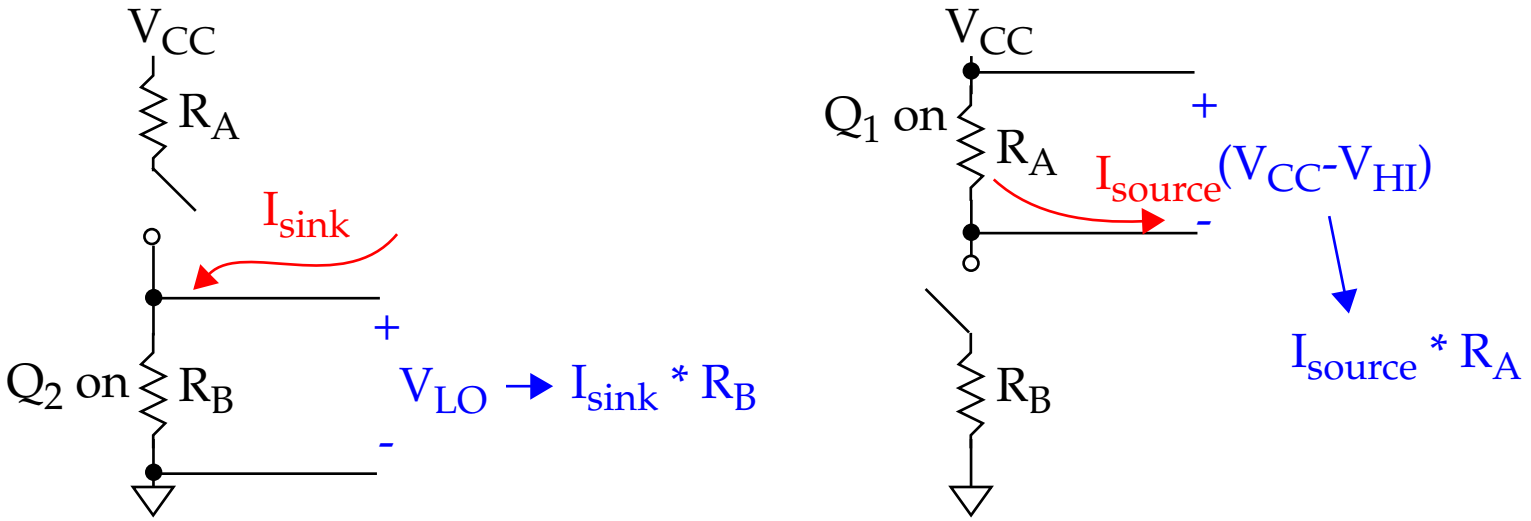
The power dissipated:

- LO state: $P = V_{LO} * I_{sink}$
- HI state: $P = (V_{CC}-V_{HI}) * I_{source}$

The ave quiescent power is: $P_{quiescent} = (0.4*I_{sink} + 1.4\ V*I_{source})/2$

Drive Circuit Dissipation

Quiescent power in **CMOS totem-pole** configuration:



The average quiescent power dissipated is the average of:

- LO state: $P_{quiescent} = I_{sink}^{2} * R_B$
- HI state: $P_{quiescent} = I_{source}^{2} * R_A$

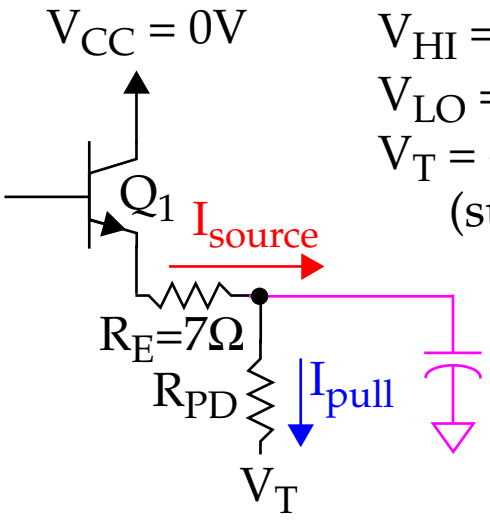
An example output spec at 25 degrees C:

- $V_{LO} = 0.15$, $I_0 = 4.0mA$ -> $R_B \sim 37$ Ohms
- $V_{HI} = 4.32$, $I_0 = -4.0mA$ -> $R_A \sim 45$ Ohms

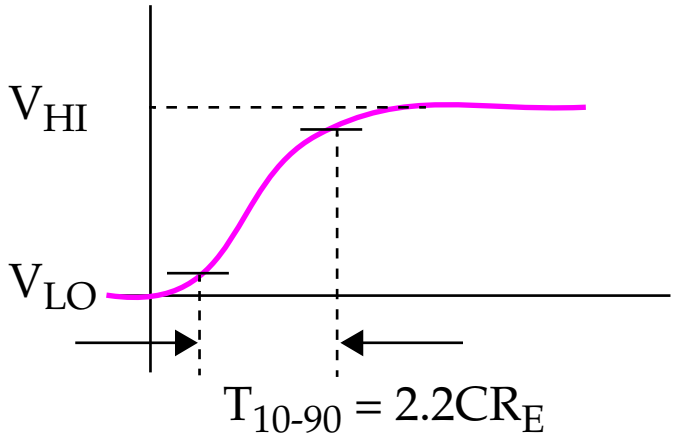
Output resistance gets larger for smaller operating voltages (2->6V possible).

Drive Circuit Dissipation

Quiescent power in ECL and GaAs **emitter follower** configuration:



V_{HI} = -0.9
V_{LO} = -1.7
V_T = -5.2 or -2.0
(supply voltage)



Quiescent power with *R* representing the Thevenin equivalent resistance in the pull-down network:

$$P_{\text{quiescent}} = \frac{1}{2}\frac{((V_{CC}-V_{HI})(V_{HI}-V_T)+(V_{CC}-V_{LO})(V_{LO}-V_T))}{R}$$

$$P_{\text{quiescent}} = \frac{1}{2}\frac{((0+0.9)(-0.9+5.2)+(0+1.7)(-1.7+5.2))}{R} = \frac{4.91}{R}$$

Note that 4.91 is for V_T = -5.2 (and it's not $\Delta V^2/R$).

Drive Circuit Dissipation

For V_T = -2.0, $P_{quiescent}$ = 0.75/R, which indicates a big power savings over V_T = -5.2.

However, the smaller current in this case also slows the fall time.

Note that emitter follower **rise time** is independent of the pull-down current.

R_E for Q_1 is given as 7 Ω in the above circuit (for 10KH ECL logic), which is much smaller than R_{PD}.

The time constant is then given as $T_{RC} = R_E*C$ (63%) and $2.2*R_E*C$ for the 10-90% transition.

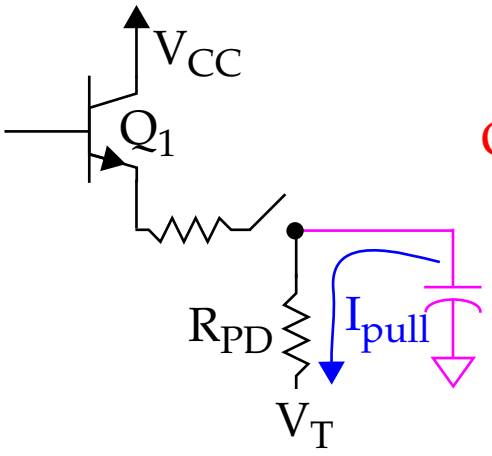
However, the turn-on time of Q_1 is usually **larger** than this time constant and therefore, dominates.

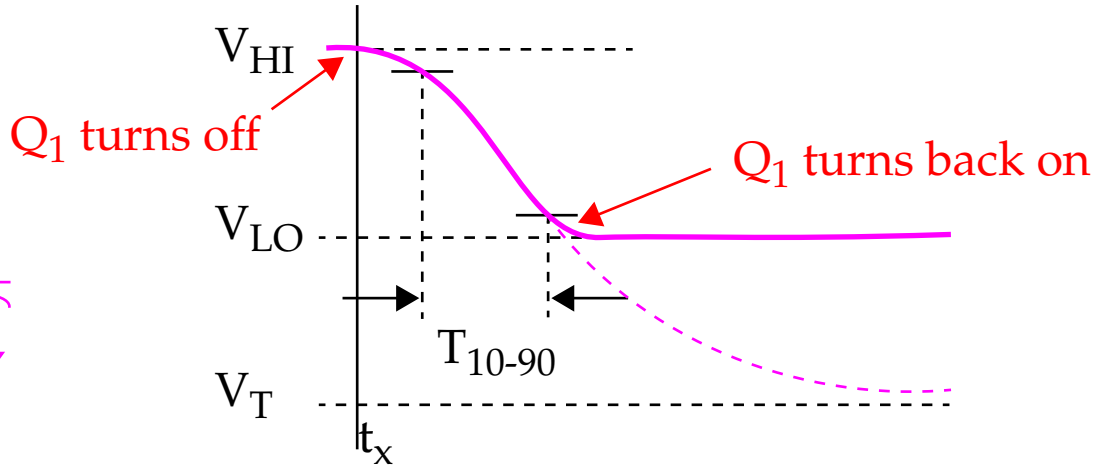
For fall time, Q_1 cuts off and R_{PD} discharges C.

Consequently, there is a trade-off between $P_{quiescent}$ and fall time, i.e. smaller values of R_{PD} improve fall time at the expense of power.

Drive Circuit Dissipation

Fall time (continued) for the emitter follower:





If Q_1 turned off instantly at the time given by t_x, then the 10-90% fall time would be:

$$T_{10-90} = R_{PD}C\ln\left(\frac{1-0.1K}{1-0.9K}\right) \qquad \text{with} \qquad K = \frac{V_{HI}-V_{LO}}{V_{HI}-V_T}$$

For V_T = -5.2V, then K = 0.186 (18.6%)

$$T_{10-90} = R_{PD}C\ln(1.179) = 0.164R_{PD}C \quad \text{vs} \quad 0.987R_{PD}C \text{ for } V_T = -2.0$$

Therefore, to equalize fall times, the V_T = -2.0 requires a smaller resistor.

Drive Circuit Dissipation

With the smaller resistor, $P_{quiescent}$ increases to the V_T = -5.2 V version!

Note, however, that once again, the turn-off time of Q_1 usually dominates.

There is *no significant advantage* in power or speed in either version -- only the resistor values are different.

One advantage of the -2.0 V version is that R_{PD} functions MUCH better as a terminator at the end of a transmission line.

Reasonable values for R_{PD} at V_T = -2.0 V are 50 Ω-100 Ω, in contrast with 330 Ω-680 Ω values for the V_T = -5.2 V version (0.987/0.164 = 6xlarger).

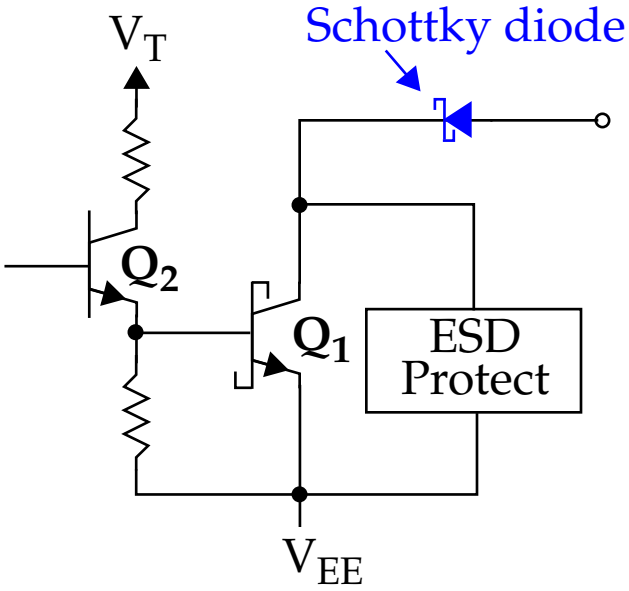
Active Power in emitter follower circuit configurations:

Dissipation in the pull-down network is usually much larger than the active power needed for charging the load capacitance.

This is also true for the *open collector* and *current source* configurations.

Drive Circuit Dissipation

Power dissipation in TTL and CMOS **open collector** configuration:



Ground or high impedance -- good for tri-state buses.

V_{HI} ~= V_T

V_{LO} = low output level

BTL (backplane transistor logic) drive circuit

Schottky diode is reversed biased when Q_1 turns off, reducing output capacitance to ~6.5 pF (lower than totem-pole which leaves a reverse biased base-to-emitter junction connected when tristated).

Quiescent power for TTL open collector (or CMOS open drain):

$$P_{\text{quiescent}} = \frac{1}{2}\frac{((V_T - V_{HI})(V_{HI} - V_{EE}) + (V_T - V_{LO})(V_{LO} - V_{EE}))}{R}$$

Output Dissipation

Power dissipated here occurs in various types of resistor termination configurations in the load itself.

Remember that power is not dissipated in ideal capacitors, so if the load is capacitive, then power is negligible.

If the load is resistive, then the power calculation is trivial.

For the high state:

$$P_{HI} = \frac{(V_{HI} - V_T)^2}{R}$$

assuming V_T is the supply voltage

For the low state:

$$P_{LO} = \frac{(V_{LO} - V_T)^2}{R}$$

Power dissipation in bias resistors is often a bigger concern than it is in the driving circuit, so care should be taken to size them to handle the worst case.