Terminations

From our previous analysis, a cable needs to be terminated when

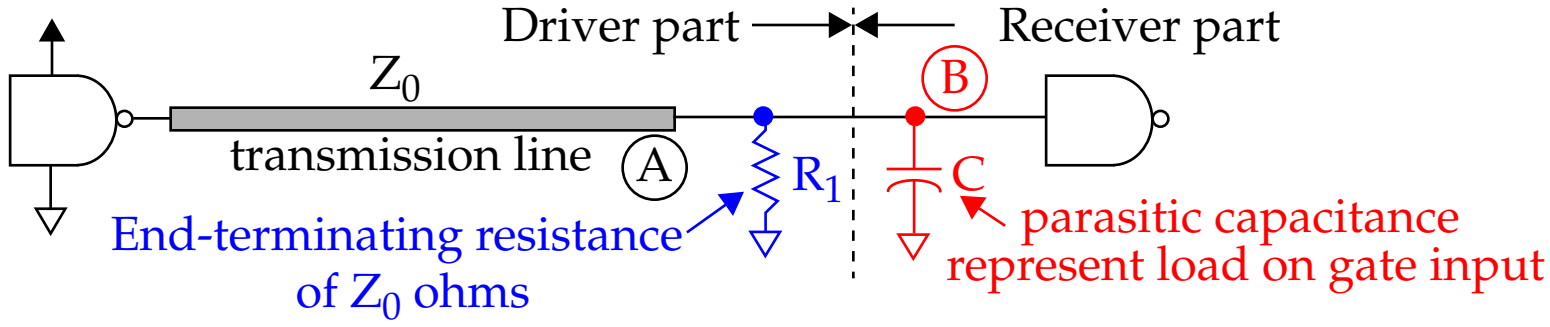
- It's long (its length exceeds 1/6 the electrical length of the rising edge) and reflections occur
- It's short (its has large inductance and drives a large capacitive load) and ringing occurs

Resistive terminations can cure both of these problems.

There are two main types:

- End terminations
- Series terminations

For **end termination**, the terminator is placed at the receiver end.



End Terminations

Characteristics:

- The driving wfm propagates at full intensity all the way down the cable
- All reflections are damped by the terminating resistor
- The received voltage is equal to the transmitted voltage

Rise time:

The Thevenin equivalent driving impedance is the transmission line impedance Z_0, in parallel with the terminating resistor (also Z_0).

This yields a drive impedance (for short term events) of $Z_0/2$.

The receiving part consists of a load capacitor (a good model for CMOS, TTL or ECL).

Therefore, this RC filter has a time constant:

$$\tau = \frac{Z_0}{2}C \xrightarrow[\text{we formulated}]{\text{previously}} T_{10\text{-}90} = 2.2\frac{Z_0}{2}C = 1.1Z_0C$$

End Terminations

The point *B* rise time is then computed from the "averaging method":

$$T_B = \sqrt{T_{10\text{-}90}^2 + T_1^2}$$

T_1 is the incoming signal rise time

This is a good model if the line is long.

When it is short (i.e., comparable to the length of its rising edge), the impedance as seen at *B* goes down.

In the limit, the driving impedance is just the output impedance of the driver. This gives a faster rise time at point *B*.

See the text for a derivation using our previous model for a transmission line:

$$S_\infty(\omega) = \frac{A(\omega)H_x(\omega)(R_2(\omega)+1)}{1 - R_2(\omega)H_x^2(\omega)R_1(\omega)}$$

An end-terminated capacitively coupled rise time is half that of a *series terminated* line (described below) under the same load conditions.

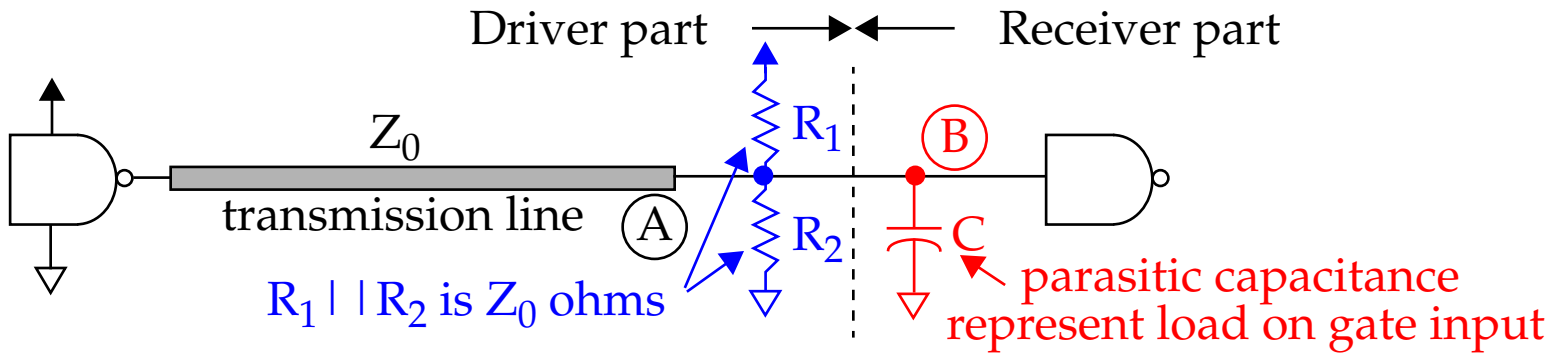
End Terminations

The termination arrangement just discussed rarely appears in TTL or CMOS circuits because of the large drive current to maintain a *high* state.

The driver must supply V_{CC}/R_1 to the terminating resistor.

With Z_0 equal to 65-Ω, a 5-V signal requires 5/65 = 76mA!

Alternatively, one can use a ***split termination***:



Here, the ratio R_1/R_2 controls the relative proportion of *high* vs *low* current.

This type of termination is sometimes used to terminate ECL circuits.

End Terminations

Setting $R_1 = R_2$ equalizes the current requirements for use with HCMOS.

If $R_2 > R_1$, *low* current exceeds *high* current, appropriate for TTL and HCT.

The selection of R_1 and R_2 can be done graphically under 3 constraints:

- The parallel combination must equal Z_0.
- We must not exceed I_{OHmax} (max high-level output current) or I_{OLmax}.

Assume **sink current** (entering the driver) is positive and **source current** is negative.

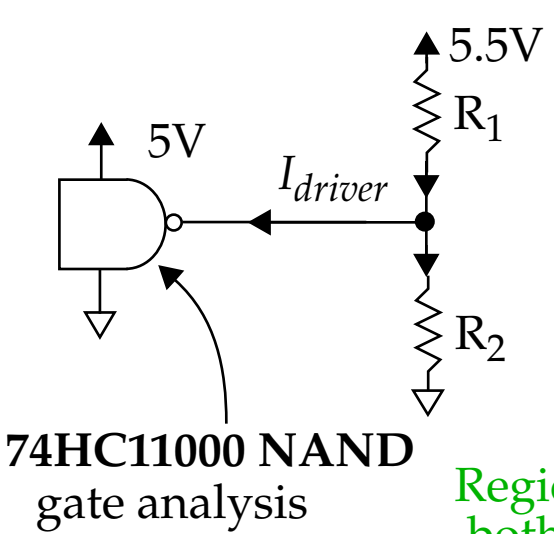
TTL and CMOS *sinks* current in *low* state and *sources* current in *high* state while ECL *sources* current in both states.

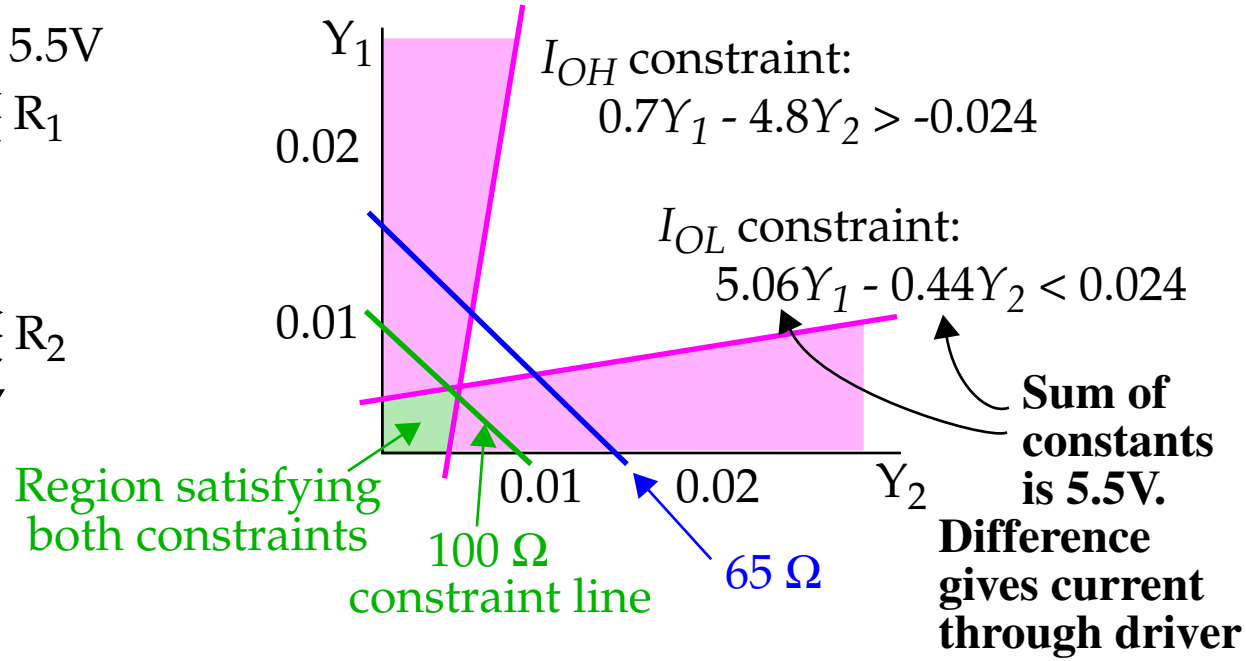
In order to keep our constraint equations linear, we use **admittances**:

$$Y_1 = \frac{1}{R_1} \quad \& \quad Y_2 = \frac{1}{R_2} \quad \Rightarrow \quad Y_1 + Y_2 = \frac{1}{Z_0}$$

End Terminations

This constraint can be graphed:





All valid combinations of Y_1 and Y_2 lie on the green and blue lines for a given Z_0.

The equations for the two other constraints is derived by noting the current that flows in the driver equals the current flowing in R_2 minus R_1.

End Terminations

These currents depend on V_{CC}, V_{EE} and the driver output voltage.

$$(V_{CC} - V_{OH})Y_1 - (V_{OH} - V_{EE})Y_2 > I_{OHmax} \qquad \textit{high} \text{ output state}$$

$$(V_{CC} - V_{OL})Y_1 - (V_{OL} - V_{EE})Y_2 < I_{OLmax} \qquad \textit{low} \text{ output state}$$

Note the left and right members of I_{OHmax} equation are negative numbers.

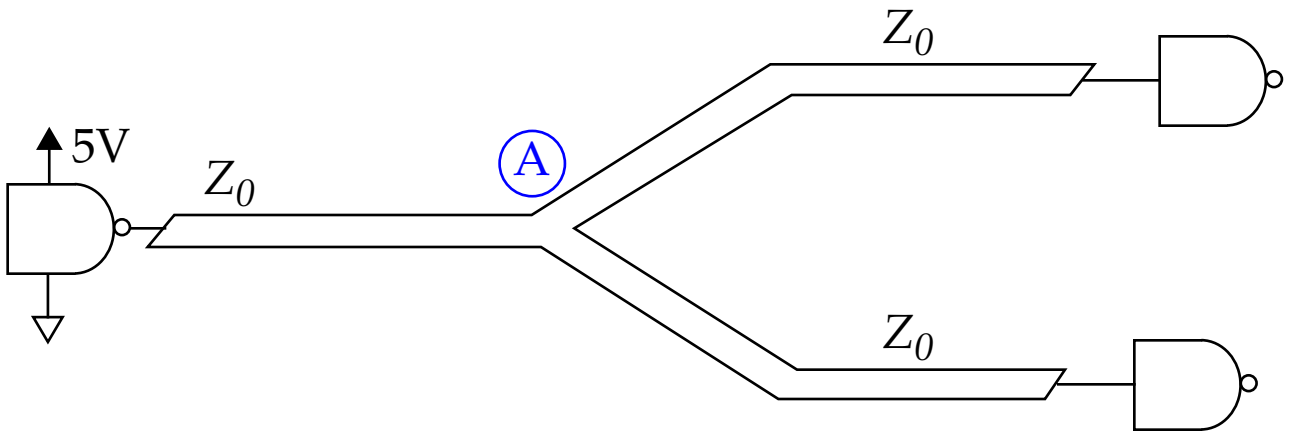
Also, the value of I_{OLmax} is a positive number for TTL and CMOS but is zero for ECL.

The 100-Ω line shown in the graph *passes* the constraint line limits and yields resistance values for R_1 and R_2 of 200 Ω.

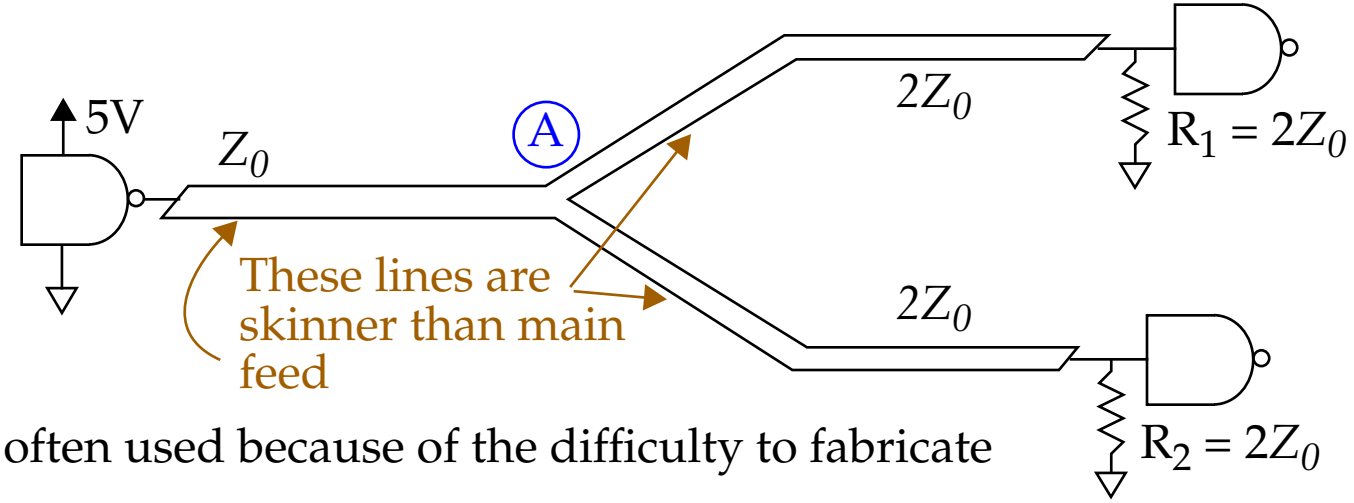
On the other hand, the 65-Ω line does not satisfy both current constraints at *any* point, and therefore cannot drive a 65-Ω load.

Other Topologies Used with End Terminations

The bifurcated line cannot be terminated properly since signal energy will always refl ects of f the junction at point *A*, causing ringing.



However, the following configuration can be properly terminated:

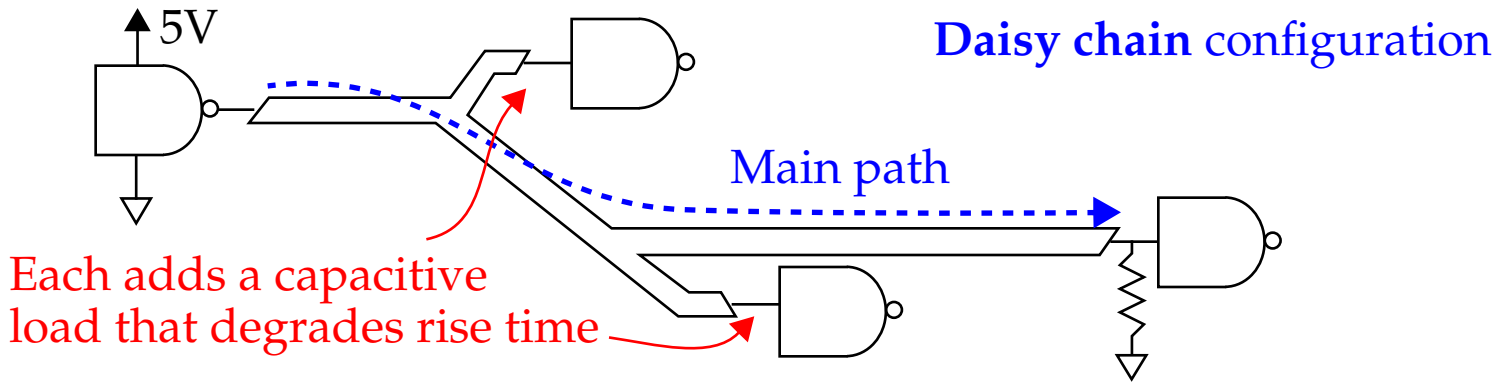


Not often used because of the difficulty to fabricate

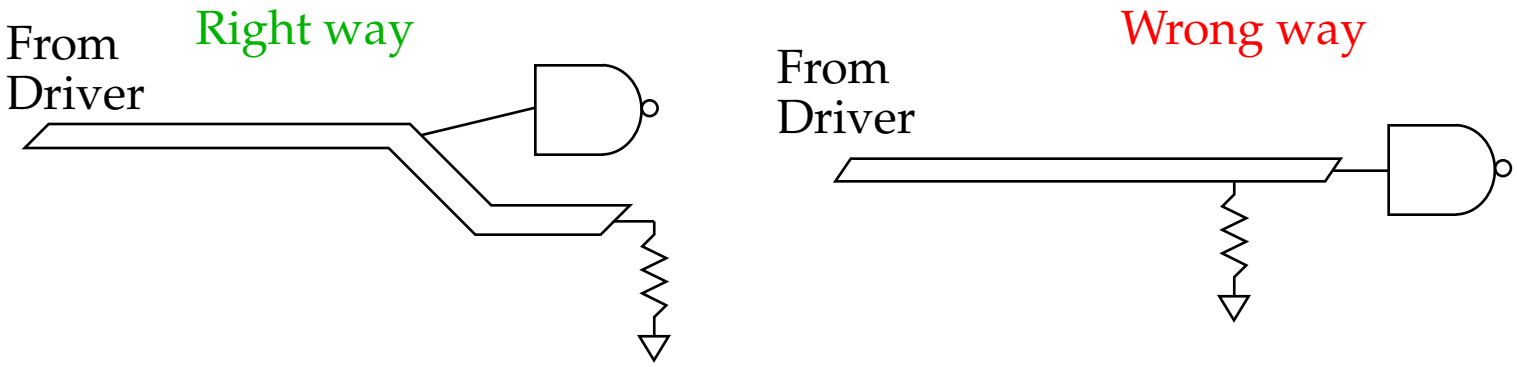
Other Topologies Used with End Terminations

End termination allows receivers to be placed at any point along the line.

Each receiver sees a delayed version of the signal.



Keep the connecting stubs short compared to the length of the rising edge to avoid refl ections at the bifurcation points.



Power Dissipation in End Terminators

Load dissipation is inversely proportional to the terminating impedance and obviously depends on the *high* and *low* operating voltages.

Under the assumption that equal amounts of time are spent in the *high* and *low* states, the power dissipated in the load resistors is given by:

$$P_{load} = \frac{(V_{HI} - V_{EE})^2 + (V_{LO} - V_{EE})^2}{2R_2} + \frac{(V_{CC} - V_{HI})^2 + (V_{CC} - V_{LO})^2}{2R_1}$$

The power dissipated in the driving circuit was discussed previously.

Source Terminators

This scheme connects the driver to the impedance line through a resistor.

The sum of the driver source impedance plus this resistor should equal Z_0 (the characteristic impedance of the transmission line).

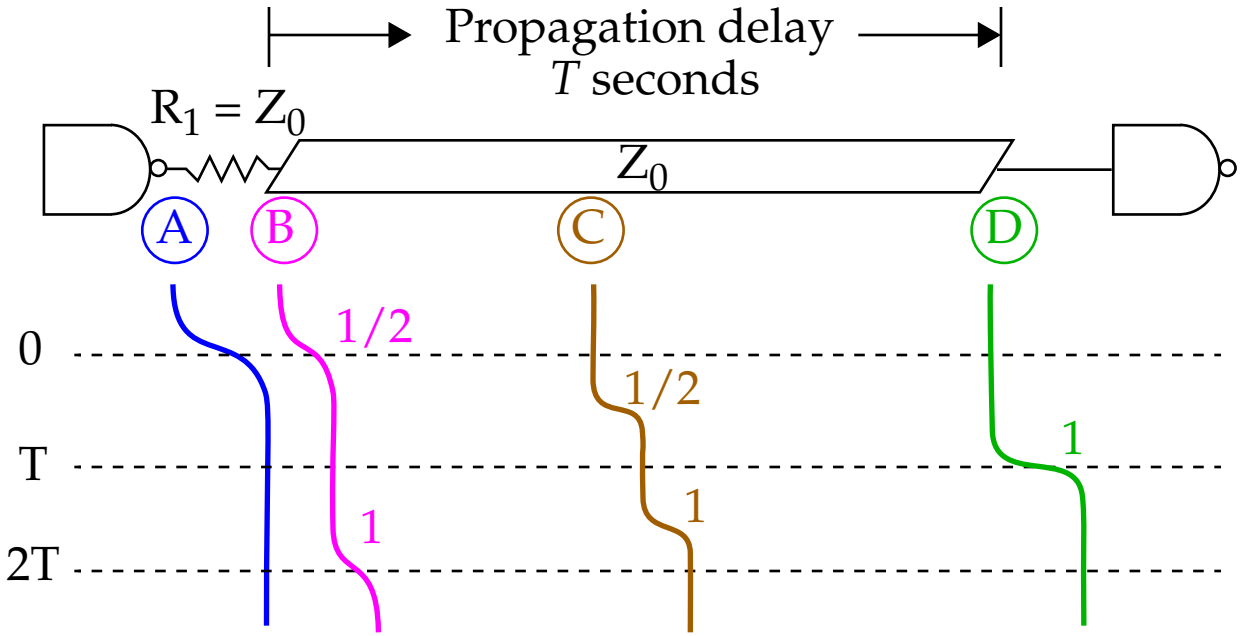
Under these conditions, the refl ection coefficient at the src is zero.

Source Terminators

Source terminated circuits have several properties:

- The drive wfm is cut in half before it begins propagating down the line.
- The driving signal propagates at 1/2 intensity to the end of the line.
- At the far end, the signal refl ection is +1 (for an open circuit).

  From previous discussions, the refl ecting half intensity signal in combination with the incoming half intensity signal restore the signal.
- The refl ected signal propagates back and damps out at the source termination (drive current becomes zero at this point).



Resistance Value of Source Termination

"Real" drivers have a small resistive output impedance (ECL is ~ 10Ω in either the *high* or *low* state).

Given the driver impedance + source terminating resistor = Z_0, the source terminating resistance is typically smaller than the line impedance.

TTL and CMOS have different output impedances in their *high* and *low* states.

Therefore, the source terminating resistance is a compromise.

From any point along the line, looking back, the drive impedance is Z_0.

For capacitive loads, we get a simple *RC* low-pass filter with time constant

$$\text{RC time constant} = Z_0 C \xrightarrow[\text{rise time}]{\text{yielding a 10-90\%}} T_{10\text{-}90} = 2.2 Z_0 C$$

Therefore, the rise time is **twice** as long as the rise time of an *end-terminated* with the same transmission line impedance and load.

Flatter Step Response of Source Termination

It is easier to eliminate reflections at the source than at the far end of a transmission line in digital circuits.

While the src has a resistive output load (plus a little inductance), the receiver usually has a capacitive load which is usually more difficult to match.

This is especially true when driving multiple loads.

Therefore, the *reflection coefficient* at the driver is more nearly **zero** than the coefficient at the receiver under end-termination.

This gives a flatter overall frequency response.

Drive Current Requirements:

The *composite* input impedance of a src-terminated line includes both Z_0 and the src-termination resistor -- sum is nearly $2*Z_0$.

The worst case drive current is:

$$\Delta V / 2Z_0$$

Drive Current Requirements by Source Termination

This worst case drive current lasts only as long as the round-trip delay.

End-terminated transmission lines require exactly the same maximum drive current if the end terminator is **biased halfway** between the logic levels.

Thus they are no more difficult to drive the *src-terminated* lines.

The input impedance of an end-terminated line is Z_0 (half that of a src-terminated line).

However, the maximum voltage difference between logic *high* or *low* and the halfway bias point is $\Delta V/2$, yielding a current:

$$\Delta V/2Z_0$$

Note that for end-terminations, adjustment of the bias point allows adjustment of the magnitude of the *high* and *low* current drive.

For src-terminations, both polarities take the same amount of current.

Other Topologies and Power Dissipation of Source Terminators

The *daisy-chain* topology does not work with src-terminators.

All loads *must* connect to the end of the line.

Loads connected midway will see the *C* wfm shown in the previous fig.

Power Dissipation (generally less than power used in end-terminated load):

The src-termination resistor has a voltage of $\Delta V/2$ impressed across it during the entire round trip delay $2T$ after switching.

During this time, the src-terminating resistor dissipates a total energy of:

$$E = 2T\left(\frac{\Delta V}{2}\right)^2 \frac{1}{R}$$

ΔV is the difference between *high* and *low*

In the case that the pulse rate is *greater* than $2T$, multiply this energy/pulse times the pulse rate to get the power dissipation.

Otherwise, assume that $\Delta V/2$ is across the resistor at all times:

$$\text{Power} = \frac{(\text{pulse freq})T\Delta V^2}{2R}$$

Middle Terminators

Systems with large fanouts and tristate drivers (a hair-ball) can result in a large amount of ringing.

The rattling lasts at least as long as the longest contiguous length in the hair-ball.

If devices in the network require monotonically rising edges, the only fix is to slow down the rising edges or filtering the received signal.

If the signal is sampled, the sampling event can be staggered to avoid the ringing.

Here, the objective is to reduce the settling time.

Four approaches to this problem:

- Add a src terminator to every driver.
- Add an end terminator at each receiver.
- Add a shunt termination in the middle of the network.
- Add series resistance between every juncture of branches.

Middle Terminators

Option 1 takes little power, provides a little bit of damping and reduces settling time.

Option 2 requires a lot of drive power but works well in **star** configurations.

A *star* has a discrete wire leading from each driver and receiver to a central point.

Refl ectionsare confined to the segment between the src and the common connection.

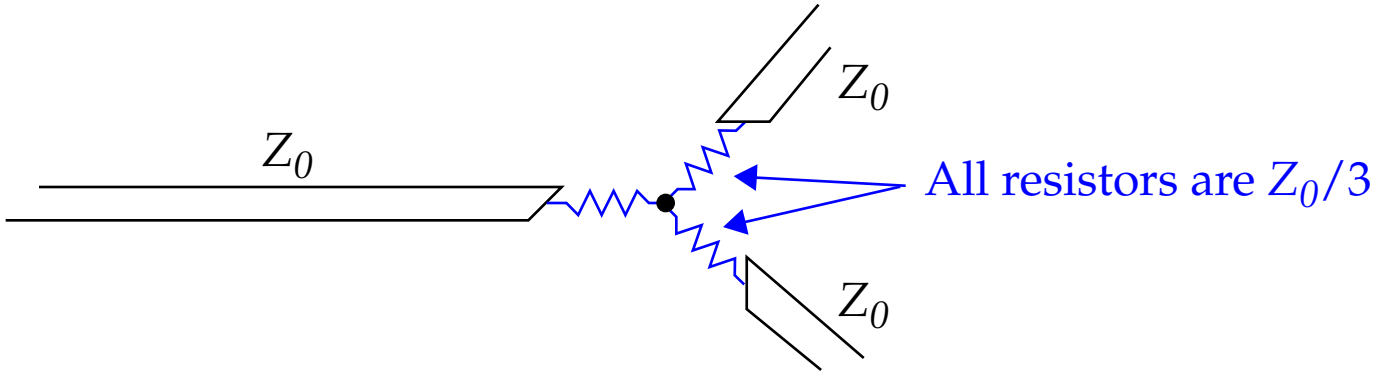
Combining options 1 and 2 wastes more power but works perfectly for *star* configurations, except that signals are attenuated through the star.

Option 3 is stupid -- don't use it. It lowers the impedance of the central part of the network where it is already too low.

Option 4 attenuates the signal at every juncture.

Middle Terminators

Option 4 (cont):



In this configuration, the signal attenuates by 1/2 as it passes through each juncture.

This damps out reflections quickly (round-trip attenuation is 1/4) but also cuts down the signal level severely as the signal traverses many of these.

Therefore, you'll need to establish an upper limit on the number of junctures you can tolerate at the receiver.