Vias

A via in a printed circuit board can be used for mounting a through-hole component or for routing traces between layers.

Electrically, both of these types have similar characteristics.

Physically, the through-hole via has a pin while the routing trace does not.

Mechanical details of vias

Smaller vias allow more routing area, and are attractive for designers concerned with product size.

Also, smaller vias have smaller parasitic capacitance, and work better for high speed products.

However, smaller vias cost more to produce.

Via diameter, pad size and spacing are the three elementary components to vias.

Mechanical Details of Vias

A through-hole via must accommodate a physical component lead.

Typical finished inside diameters range between 0.010 to 0.028 in.

Not much can be done to reduce this.

For trace routing, the required finished diameter is constrained by drilling and plating technology.

Smaller holes require smaller drill bits, which tend to break more often than big ones.

Electroplating does not penetrate a deep, skinny hole.

Holes deeper than 6 times their diameter will not plate uniformly, which limits hole diameters to 0.010 in. for standard boards 0.063 in. thick.

Mechanical Details of Vias

Every via requires additional space for a pad and for clearance around the pad.

The pad electrically connects the plated interior of the via to the traces on the surface or within the board.

The appropriate size of the **pad** is determined by four factors:

- Plating allowance
- Hole diameter tolerance
- Hole alignment allowance
- Required annular ring

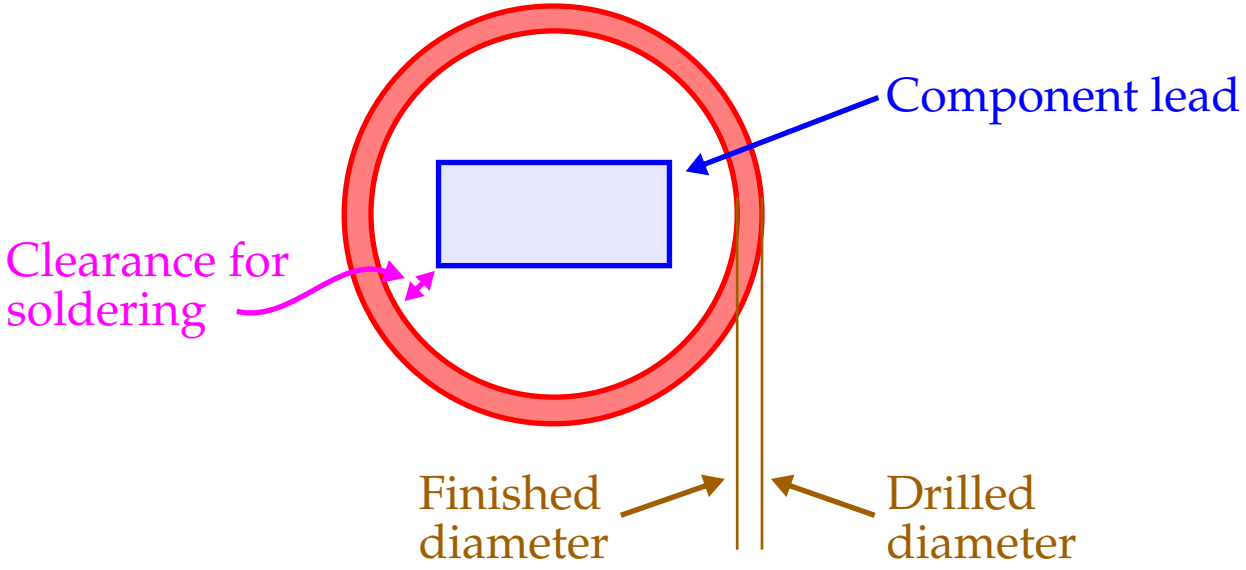
A via is drilled and then plated.

Plating coats the interior of the hole and builds up a conductive surface about 0.001-0.002 in. thick, making the diameter 0.002-0.004 smaller.

The difference between the drilled hole size and the maximum plating thickness is *plating allowance*.

Mechanical Details of Vias

It follows that the *plating allowance* is twice the maximum plating thickness.



Holes are drilled with a *hole diameter tolerance*, e.g., 0.032 +- 0.003 in.

However, a small hole with variation that makes it smaller is not acceptable.

Therefore, the *nominal* hole size is increased slightly to prevent this.

This oversizing adds to the *plating allowance* (given above).

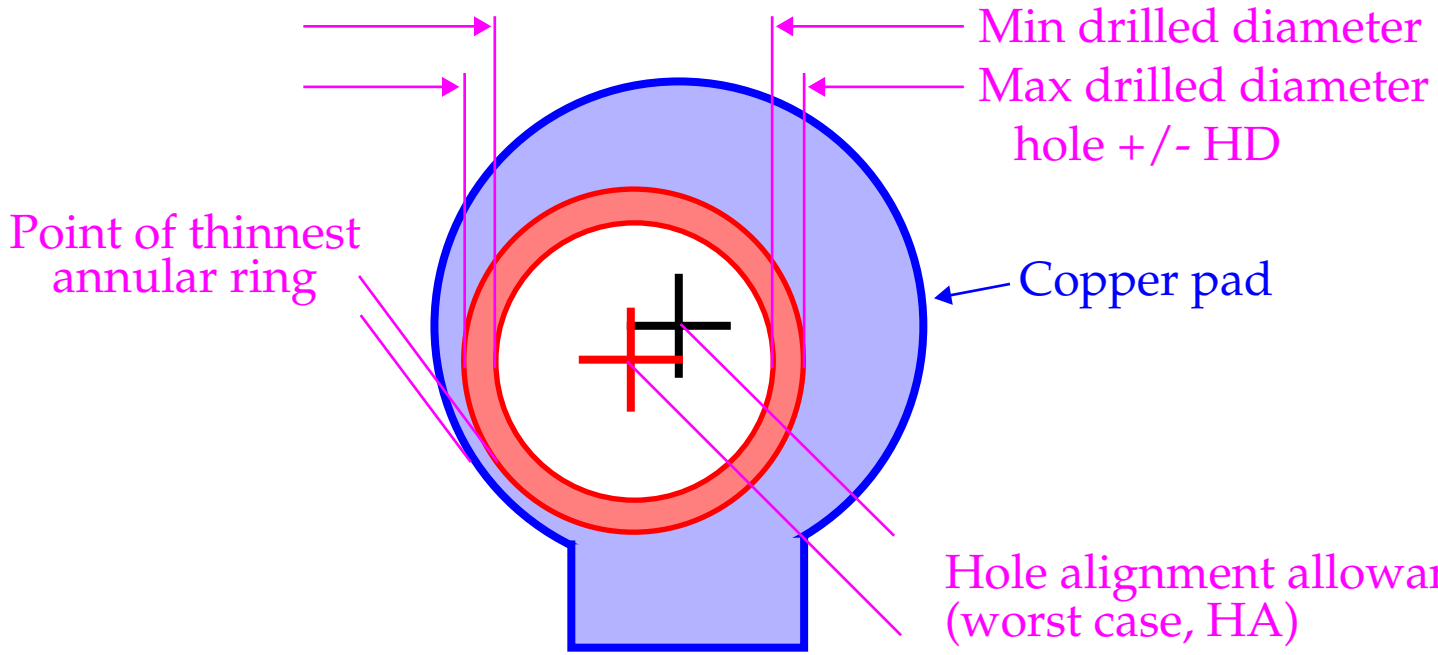
Mechanical Details of Vias

The *hole alignment allowance* accounts for error in the drilling location.

The drilling machine attaches to special **reference holes** provided on the board, which are also used during the etching process for alignment.

The manufacturer specifies a hole alignment allowance which specifies the level of error in the drilled holes from the *nominal etched pad centers*.

It includes both drilling and etching alignment errors.

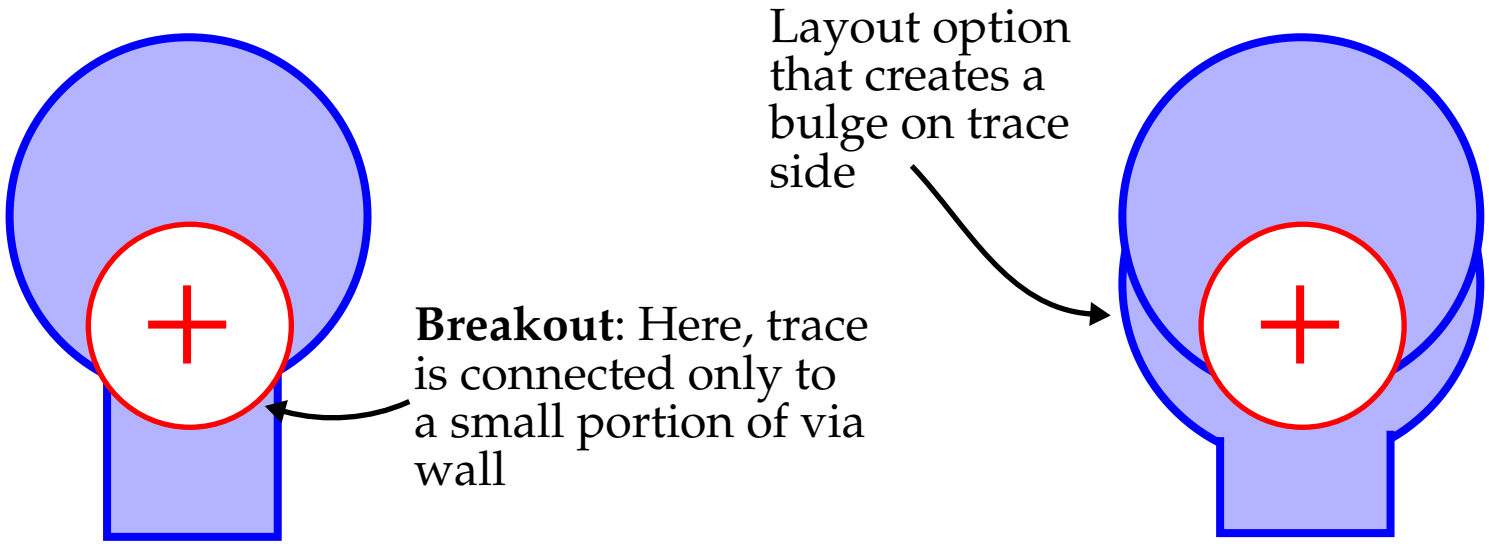


Mechanical Details of Vias

A hole that is drilled off center may **break through** the annular ring, a condition called *breakout*.

If it occurs on the trace side of the pad, it can jeopardize electric contact between the trace and the interior portion of the via.

The *required annular ring* specifies the minimum amount of copper pad surrounding the via under *worst-case drilling*.



Mechanical Details of Vias

The minimum pad diameter, PD, can be calculated as:

PAD = FD + PA + 2(HD + HA + AR)

FD: required min. finished hole diameter

PA: plating allowance

HD: hole diameter tolerance

HA: hole alignment allowance

AR: annular ring required

And the correct *nominal* drilled hole diameter is:

HOLE = FD + PA + HD

Clearance Requirements: Air Gap

The space between copper features on a PCB is called an *air gap*.

For digital applications, only a small air gap is needed to prevent arcing.

Here, solder bridges are much more common mode of failure.

Clearance Requirements: Air Gap

Imperfections in the etching process cause solder bridging, that occurs during assembly.

The minimum safe clearance that prevents solder bridges depends on:

- Precision of the etching process
- Assembly method
- Required yield

The manufacturer will have a *line width tolerance*, which defines the precision.

Subtract this value from the *nominal air gap* when calculating the worst case clearance.

Each feature extends a maximum of 1/2 the line width tolerance (reason for subtracting it only once).

Wave soldering (wave of solder passed over board) and **reflow soldering** (solder paste heated) are the two major types of assembly processes.

Wave soldering is more prone to solder bridges.

Clearance Requirements: Air Gap

Through-hole soldering always uses wave soldering.

Surface mount boards can use either or both.

With regard to yield, the requirements here depend on volume and cost.

At low volumes, you may choose to perform a visual inspection to remove any solder bridges.

At high volumes, it is better to spend extra design effort on locating and fixing clearance problems.

Note that both etching imperfections and solder bridges are random phenomena.

Increasing air gaps reduces their probability but never completely eliminates them.

Trace-Routing Density Vs. Via Pad Size

PCB cost is proportional to the number of layers and the number of layers depends on the wiring density of each layer.

Wiring density is measured in units of *average trace pitch*, with trace pitch defined as the minimum center-to-center spacing of two traces.

Wiring density is influenced by the number of vias.

The number of traces that fit between adjacent vias is called the number of *tracks*.

Via spacing impacts the *average trace pitch*.

Via spacing is usually confined to a grid, at 0.100 for through hole designs and lower, e.g., 0.050, for surface-mount designs.

Via Capacitance

Vias have parasitic capacitance to ground that behaves like a *lumped* capacitance.

Via Capacitance

The following formula approximates (within an order of magnitude) via capacitance, assuming there is a pad on each layer.

$$C = \frac{1.41\varepsilon_r T D_1}{D_2 - D_1} \quad \text{in pF}$$

with D_2 = diameter of clearance hole in ground plane.

D_1 = diameter of pad surrounding via

T = thickness of PCB

ε_r = relative electric permeability of the circuit board material

One way to reduce capacitance is to shrink or eliminate pads on ground layers and other layers not connecting to the via.

A typical value for a via is 0.5 pF.

This has a small impact on the rise time of a 50 Ω transmission line.

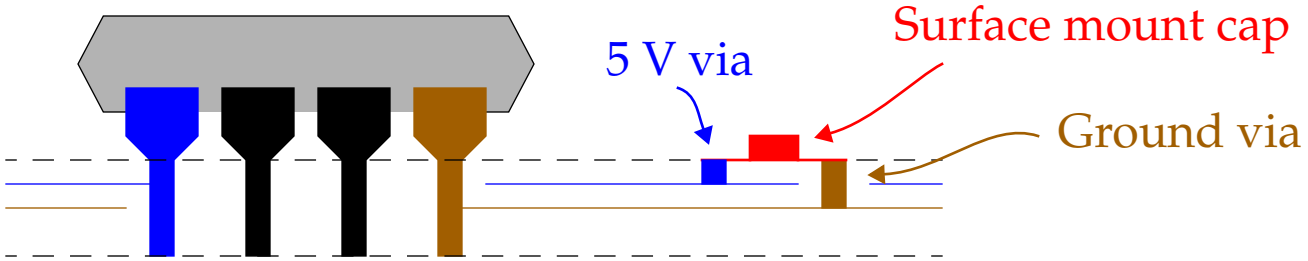
$$T_{10\text{-}90\%(\text{step response})} = 2.2C\left(\frac{Z_0}{2}\right) = 27.5 \text{ ps}$$

Via Inductance

Parasitic series inductance usually has a larger impact than parasitic capacitance.

They have an adverse impact on power supply bypass capacitors.

Bypass capacitors are designed to short together, at high frequencies, two power planes.



The vias used to connect the power and gnd planes to the bypass cap have a measurable inductance approximated by.

$$L = 5.08h\left[\ln\left(\frac{4h}{d}\right)+1\right] \qquad \text{in nH}$$

h = height of via, in.

d = diameter of via.

Via Inductance

The *ln* within this equation indicates that changing via diameter does little to influence the inductance.

However, reducing length has a much larger impact.

For example, given $h = 0.063$ in., $d = 0.016$ in. and $T_{10\text{-}90} = 1$ ns.

$$L = (5.08)(0.063)\left[\ln\left(\frac{4(0.063)}{0.016}\right) + 1\right] = 1.2 \text{ nH}$$

$$X_L = \frac{\pi L}{T_{10\text{-}90}} = 3.8\ \Omega$$

Bear in mind that this resistance occurs on the V_{DD} side as well, doubling the impact.

Adding bypass capacitors in parallel reduces this effect as long as they are within a radius of $l/12$, where l is the electrical length of the rising edge.

This ensures they all act in concert as a lumped element.

In FR-4, 1 ns has a length of about $l = 6$ in., setting $l/12$ to 0.5 in.

Via Inductance

Power supply bypassing gets more difficult as rise times get shorter.

The number of caps within the effective radius shrinks with the **square** of the rise time.

Also, the inductive reactance of the via goes up (for higher frequencies), making this even worse.

For example, a bypass configuration that works well at one frequency is **eight** times *less effective* when we halve the rise time.

Return Current and its Relation to Vias

In multi-layer boards with more than one ground plane, the path taken by the return current is important to consider.

Recall that high-speed return signal currents follow the path of *least inductance.*

Return Current and its Relation to Vias

The scenario that introduces problems when using multiple ground planes is when the signal trace changes layers.

Here it is possible that the ground return current is NOT able to switch ground planes, and therefore, the loop and inductance increase.

Some rules of thumb:

- Don't wire your board so that the return currents for high speed traces have to jump between planes, i.e., keep the signal traces on the same plane.

- Restrict traces to remain on **either side** of whichever ground plane they start out nearest.

  This allows two trace planes (one vertical and one horizontal) to be used to get signals to their proper places.

- Put ground vias next to every signal via to allow return currents to jump if needed.

- Add lots of extra ground vias to reduce the diversion of return currents.

Return Current and its Relation to Vias

Do **not** use guard traces to provide a nearby return-current path.

Guard traces are not effective unless they are very close to the signal trace.

Once they get close enough, they mess up (lower) the trace impedance.

Also, in order to provide a low enough impedance, guard traces must be VERY wide to make any difference.