CounterMeasures I(A)

Multiple choice:
1) Time dimension countermeasures are designed to
a) Manipulate the clock to make it difficult for the attacker to synchronize to the clock signal
b) Add parallelism to the algorithm's execution
c) Running random number generations
d) Make it difficult for the attacker to synchronize with an algorithm's execution

2) Amplitude dimension countermeasures are designed to
a) Increase the signal and/or decrease the noise in the power traces
b) Reducing the signal and/or increase the noise in the power traces
c) Randomize the instructions
d) Randomize the clock

CounterMeasures I(B)

Multiple choice:
1) Cell level countermeasures are classified as dual rail precharge (DRP) logic styles which means
a) The gates are defined using differential resistant pass gate logic
b) The circuit computes a differential logic function which adds noise
c) True and complimentary wires are used to define connections between logic gates and the circuit operates in two phases, precharge and evaluate
d) The logic gates are defined using two power supplies which confuses the adversary about which rail is actually being used

2) Why is it necessary to balance the output capacitive loads in DRP logic styles?
a) To prevent the adversary from deciding whether the true or complementary wires are being switched
b) To maintain the clock specification
c) To minimize power consumption
d) To reduce the noise levels because of signal reflections that occur because of mismatch

CounterMeasures I(C)

Multiple choice:
1) The characteristics of Sense Amplifier Based Logic (SABL) logic include all of the following except
a) All internal nodes in the DPDN are connected to one of the four output nodes
b) All internal nodes are cross-coupled through capacitive loading
c) All conducting path have the same resistance
d) A conducting path through the DPDN cannot occur until all input signals have arrived and have settled

2) The characteristics of Wave Dynamic Differential Logic (WDDL) logic includes all of the following except
a) Both of the functions within a WDDL gate are inverting
b) Both the functions within a WDDL gate are positive monotonic
c) Only one of outputs q or q_bar switches from 0 to 1 during evaluate
d) During precharge, all input nodes are set to 0