Time and Frequency Domain Transient Signal Analysis for Defect Detection in CMOS Digital ICs

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Abstract

A novel approach to testing CMOS digital circuits is presented that is based on an analysis of voltage transients at multiple test points and I_{DD} switching transients on the supply rails. We present results from hardware experiments which show distinguishable characteristics in the transient waveforms of defective and non-defective devices. These variations are shown to exist in both the time domain and frequency domain for CMOS open drain and bridging defects, located both on and off sensitized paths.

1.0 Introduction

Transient Signal Analysis (TSA) is a new parametric approach to testing digital integrated circuits. Defect detection is accomplished in TSA by analyzing the transient signals of a device measured simultaneously at multiple test points. The transient waveforms characterize the physical components of the device. Signal variations between devices result primarily from changes in the resistive, inductive and capacitive components of the coupling network, as well as in the gain and threshold voltage characteristics of the transistors. Variations in the values of these circuit parameters may result from process tolerances, or they may result from defects.

The approach has two advantages over other logic and parametric testing methods. First, by analyzing small signal variations in the transient waveforms, TSA can detect the presence of defects at test points that are not on logic signal propagation paths from the defect site. This is possible because of the device coupling mechanisms which include the resistive and capacitive coupling through the power supply and the wells, as well as parasitic capacitive and inductive coupling between conductors. The large signal variations of faults at defective nodes couple through adjacent conductors and produce small signal variations at test point nodes. The ability to detect defects without requiring their faults to be propagated to observation points improves the sensitivity of the device test and may reduce the test set generation size and complexity.

The second advantage of TSA is the use of multiple test point signals. By cross-correlating the

signals measured simultaneously at different topological locations on the device, it is possible to distinguish between signal variations caused by process tolerances and those caused by defects. This is true because process tolerance effects tend to be global, causing signal changes on all test points of the device. In contrast, signal variations caused by a defect tend to be regional and more pronounced on test points closest to the defect site.

In this paper, we present the results of four hardware experiments conducted on devices with bridging and open drain defects. We demonstrate the regional and global signal variations that occur in the test devices by measuring the voltage transients at a set of test points located on probe pads on the surface of the die. We introduce **Signature Waveforms** or **SWs** as a means of capturing signal variations in both the time and frequency domain representations of the test point waveforms. We show that the fourier phase components of the frequency domain SWs posses better discriminatory information than the magnitude or time domain SWs.

The remainder of this paper is organized as follows. In Section 2, we present related research on device testing. Section 3 describes Signature Waveforms. Section 4 presents the results of hardware experiments conducted on devices with intentionally inserted bridging and open drain defects. Section 5 gives a summary and conclusions.

2.0 Background

Parametric device testing strategies [1][2] are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of quiescent supply current or transient response. Parametric methods have been shown to be more effective than conventional logic based methods in detecting common types of CMOS defects [3][4]. Many types of parametric tests have been proposed [5] but recent research interest has focused primarily on three types; I_{DDQ} [6], I_{DD} [7], and delay fault testing [8][9].

I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value [10]. I_{DDQ} has been shown to be an effective diagnostic technique for CMOS bridging defects, but is not applicable to all types of CMOS defects [11]. Recently, concerns have been raised over the applicability of IDDQ to deep sub-micron technologies [12].

Several dynamic supply current I_{DD}-based approaches have since been proposed

[7][13][14][15][16]. In general, these I_{DD}-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as I_{DDQ}, however, circuit size and topology are still factors that affect the defect resolution of these schemes. Also, these methods do not provide a means of accounting for process tolerances and are therefore subject to aliasing problems.

Alternatively, delay fault testing takes advantage of the fact that many CMOS defects cause a change in the propagation delay of signals along sensitized paths [4]. Difficulties with delay fault testing include the complexity of test generation and path selection [17][18]. More importantly, Pierzynska and Pilarski have shown that a non-robust test can detect a delay fault undetectable by any robust test [19]. Franco and McCluskey [20] and others [21][22][23] have proposed extensions to delay fault testing that address some of these difficulties.

Recently, Ma, *et al.* [24] and others [3][4][25][26] evaluated a large number of test methodologies and determined that a combination of several test strategies may be necessary in order to find all defective devices. In particular, Ma, *et al.* discovered that I_{DDQ} cannot detect all kinds of defects and must be used with some kind of dynamic voltage test. Our technique, Transient Signal Analysis (TSA), with its advantages in defect detection and process insensitivity, is proposed as an addition to this test suite.

In previous papers [27][28], we have demonstrated through simulation experiments that global variations of major device performance parameters, i.e. threshold voltage and gate oxide thickness, result in measurable changes of the circuit's transient response at all test points. In contrast, the presence of a device defect will change both the value and topology of the parasitic components in the region of the defect. We have shown through other simulation experiments that the changes introduced by both of these classes of defects result in measurable variations in the transient response and that these variations are distinct at two or more test points.

3.0 TSA Procedure

TSA is based on the analysis of transient signal variations. In order to capture the variations produced by defects in the test point signals, we create Signature Waveforms using the procedure shown in Figure 1. Shown in the upper portion of the left plot of Figure 1 are the transient waveforms generated by two devices at a test point located along a sensitized test path. Simi-

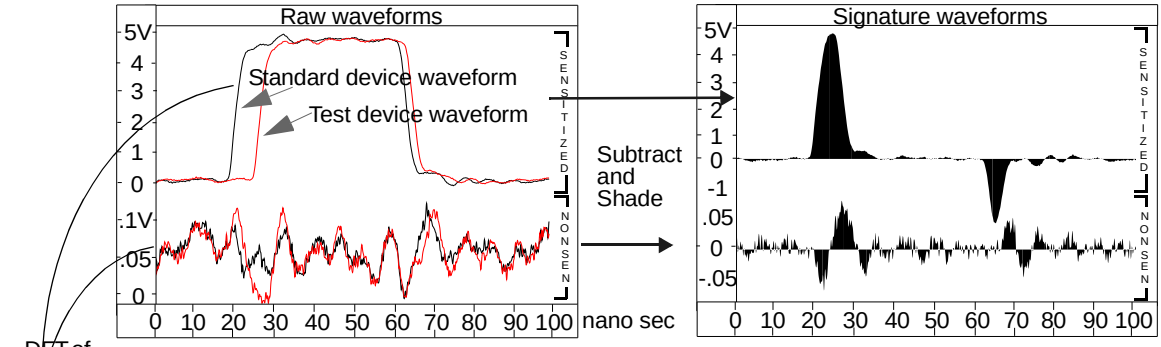

Figure 1. Time Domain Signature Waveform creation procedure.

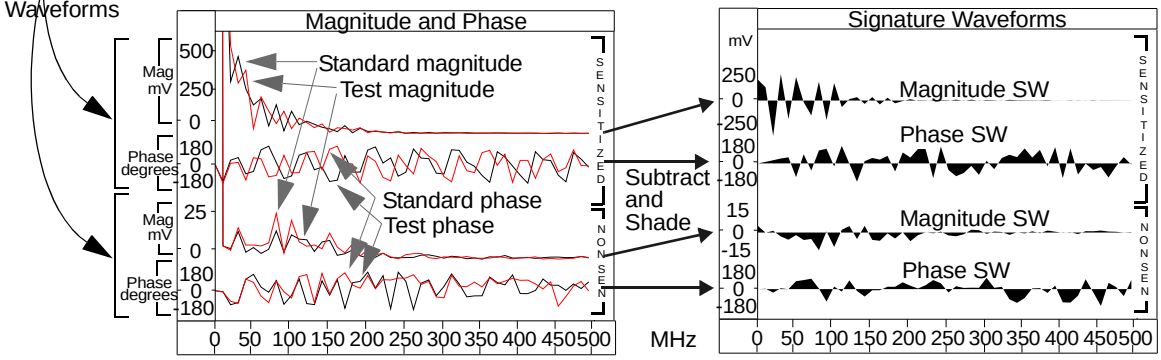

Figure 2. Frequency Domain Signature Waveform creation procedure.

larly, shown along the bottom are two transient waveforms produced by the same two devices at a non-sensitized test point. Signature Waveforms (SWs) are created from these pairs of transient waveforms by subtracting the test device waveform from the standard device waveform. The difference waveforms, shown in the right plot of Figure 1, are shaded along a zero baseline to add emphasis to the variations. The frequency domain SWs are created by performing a discrete fourier transform (DFT) on the raw time domain waveforms as shown in Figure 2. Magnitude and phase SWs are created by subtracting the test device magnitude and phase values from the corresponding values of the standard device.

4.0 Experimental Design

In this section we present the results of several hardware experiments designed to demonstrate that it is possible to characterize ICs using time and frequency domain Signature Waveforms. We designed three versions of the ISCAS85 c432 benchmark circuit [29], a version with intentionally inserted bridging defects, a version with intentionally inserted open drain defects and a defect-free version. Four devices of each version were fabricated at MOSIS using ORBIT's 2.0µm SCNA process. The defect-free devices were verified using both functional and Stuck-At

test sets.

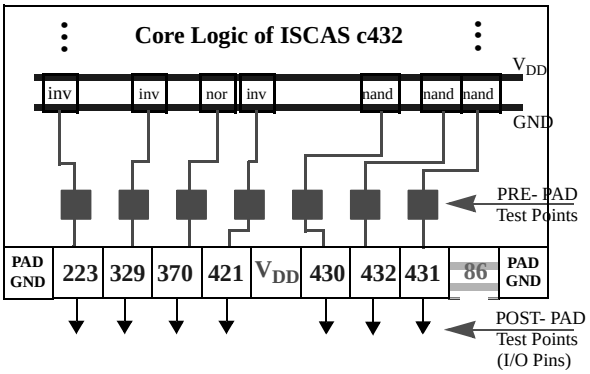

Figure 3. Location of the test points on the c432.

The test points used in these experiments are labeled PRE-PAD and POST-PAD in Figure 3. The reader is directed to reference [30] for a discussion of the POST-PAD results. The PRE-PAD test points are 22 micron square Metal 2 pads placed on the output nodes of the gates driving the seven primarily outputs of the c432. Since the test points are driven directly by the core logic, variations introduced through coupling mechanisms in the I/O pads are reduced. Moreover, core logic test point measurements eliminate signal attenuation effects introduced by the I/O pad drivers. The measurements were taken at a probe station using a PicoProbe, model 12C, with a 100 FF and 1 MΩ load.

The TSA testing process involves applying a test vector sequence to the primary inputs (PIs) of an IC and sampling the waveforms generated at the test points. Signature Waveforms extract only the variation that occurs between the test devices and the standard device. In each experiment four defect-free and four defective devices were tested. The same defect-free standard device was used in all experiments.

4.1 Bridging and Open Drain Experiments

We report the results of the first bridging defect experiment and summarize the results of the other experiments. We analyze only the SWs of off-path test points in these experiments and demonstrate that the signal variations caused by defects are most easily measured as phase shifts in the frequency domain SWs.

Figure 4 shows a portion of the schematic diagram of the c432. The input stimulus for this experiment toggles PI 66 at 11MHz. PI 56 is held high and the other PIs (not shown) are held low.

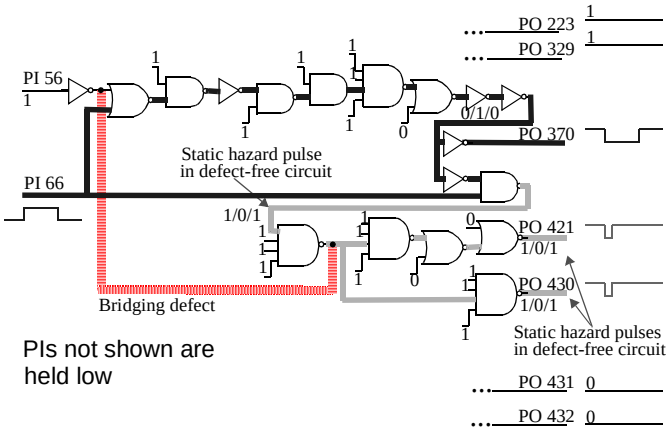

Figure 4. Portions of the c432 schematic showing the short and the sensitized paths affected by the defect of Bridging Experiment #1.

The dotted line in the figure represents the bridging defect which was created in the layout by inserting a first-level to second-level metal contact between the output lines of the 4-input NAND and the inverter. The only PO that changes logic state is 370. However, in the defect-free circuit, a static hazard causes a pulse to propagate to POs 421 and 430 along the shaded paths shown in the figure. Note that the bridging defect is not on any sensitized path and no contention exists between the two bridged nodes in steady-state. However, since the output of the inverter driven by PI 56 is low, the bridge eliminates the pulse produced by the hazard in the defective devices. The large signal variation caused by the removal of the hazard couples into adjacent nodes. We demonstrate that it is possible to use the transient signals of non-sensitized test points 223, 329, 431 and 432 to identify the defective devices.

Each of the rows of plots in Figure 5 shows a set of time domain and frequency domain SWs from a single test point identified in the header. The time domain SWs are shown in the left-most plots while the magnitude and phase SWs are shown in the middle and right-most plots respectively. The top-most waveform of each plot is the output trace from the standard defect-free IC used in the difference operation to create the SWs shown below it. The next three waveforms labeled DF#*x* are the SWs from each of the three remaining *Defect-Free* ICs. The next four SWs, labeled either BR#*x* for *BRidging* defects or OD#*x* for *Open Drain* defects, are the SWs from the four defective ICs. Given that our objective is to identify defective devices using these waveforms, this format facilitates the comparison of the set of defect-free device SWs with the set of defective device SWs. The discussion that follows focuses on identifying distinguishable charac-

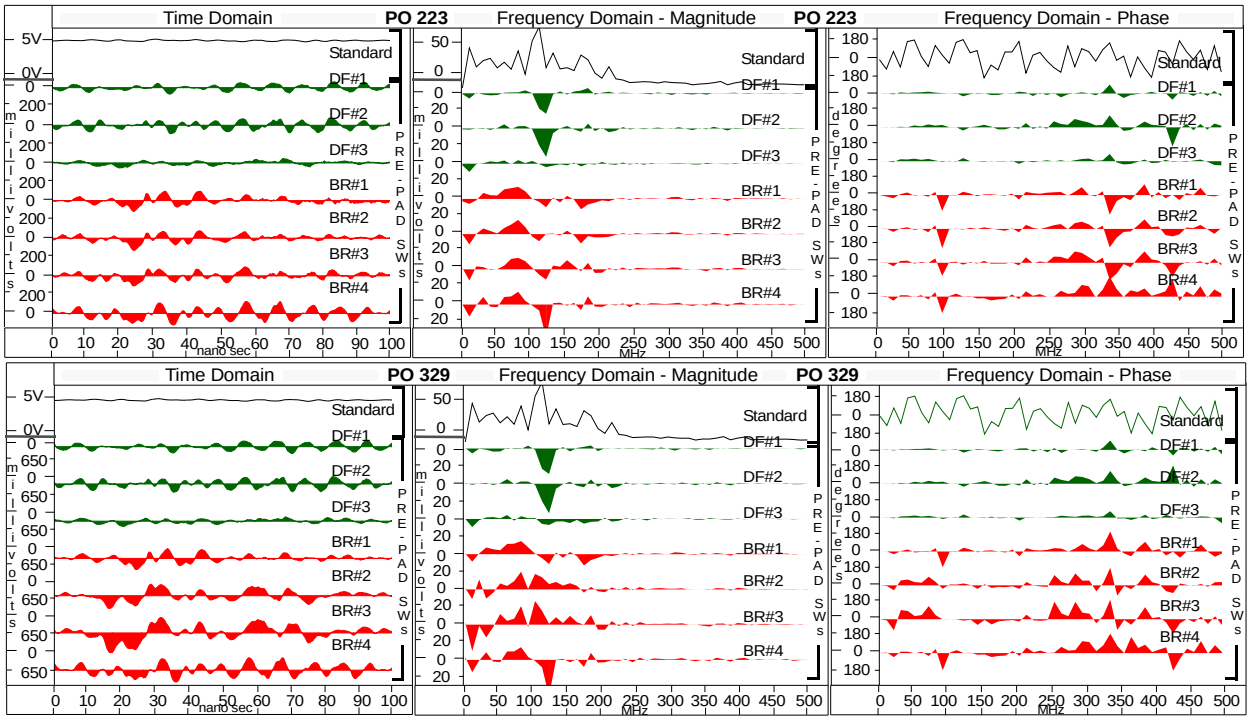

Figure 5. Time and Frequency domain Signature Waveforms from POs 223 and 329 of Bridging Exp. #1.

teristics that occur in one set and not in the other.

As indicated in the schematic diagram of Figure 4, POs 223 and 329 remain steady-state high under the test sequence. The time and frequency domain SWs for these test points are shown in Figure 5. The most significant distinguishable characteristic that occurs between the sets of defect-free and defective SWs in the figure is illustrated in the Phase plots on the right. In this case, phase shifts occur in the BR#1 and BR#4 SWs at 100 MHz and between 10 and 100 MHz in the BR#2 and BR#3 SWs. No significant variation occurs in the phase SWs of the defect-free devices below 250 MHz. The Magnitude SWs of the defective devices shown in the middle plots of these figures also show distinguishable variation in the region between 50 and 100 MHz. But the variation in the magnitude SWs of DF#1 and DF#2 at 125MHz create an anomaly in the characterization of the defect-free devices. However, this anomaly can be attributed to process tolerances if the Magnitude SWs of POs 223 and 329 as well as POs 431 and 432 (Figure 6) are considered together. This is true because the variation is global in that it occurs at the same frequency and with the same relative magnitude in all four test point SWs. In summary, these results indicate that the defect delays and distorts specific frequency components of off-path signals. This phenomena is difficult to see in the time domain SWs of Figure 5 because other fre-

quency components combine to mask these variations.

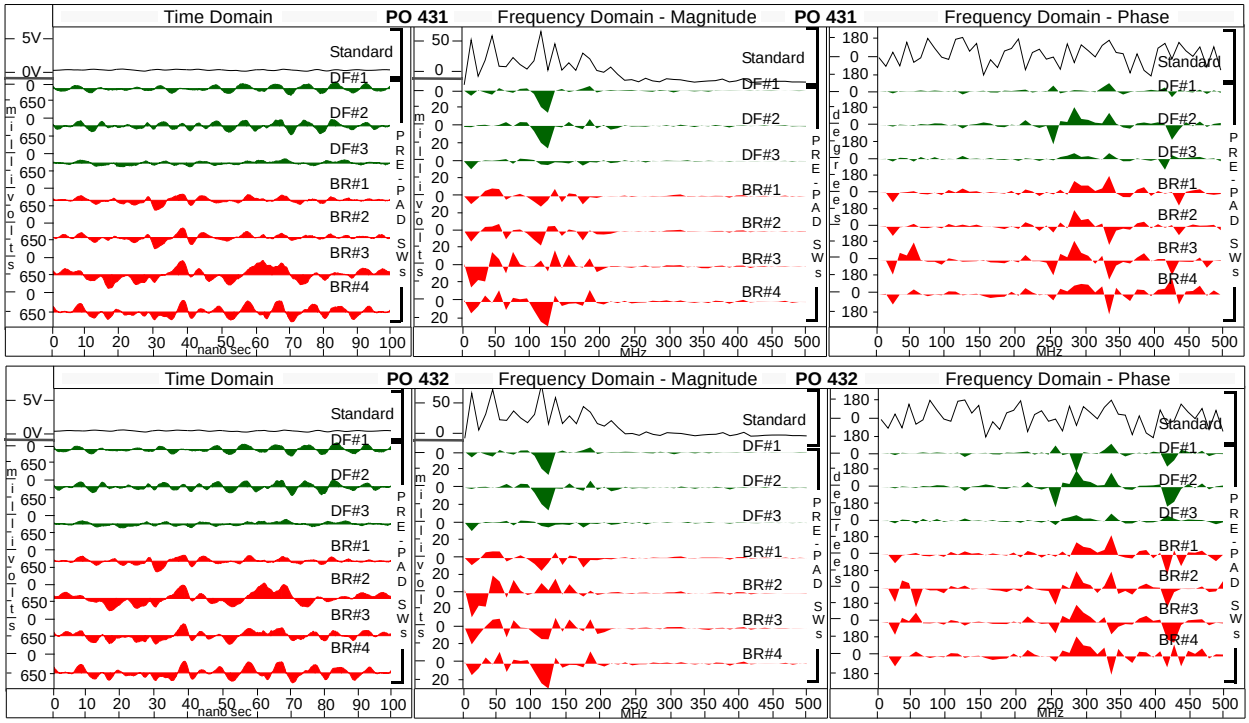

Figure 6. Time and Frequency domain Signature Waveforms from PO 431 and 432 of Bridging Exp. #1.

The SWs for POs 431 and 432 are shown in Figure 6. POs 431 and 432 remain at steady-state low under the test sequence Again we note specific phase shifts and distortions of magnitude in the Phase and Magnitude SWs of the defective devices while the time domain SWs are nearly indistinguishable. More importantly, however, is the change in the frequency range of the phase shift in these outputs when compared with POs 223 and 329. In this case, the phase components between 15 and 20 MHz have been shifted by the defect. Unlike the variation caused by process tolerances observed in all Magnitude SWs of devices DF#1 and DF#2, the difference in the phase behavior between these two sets of outputs suggests that this variation is due to a defect since it is different depending on the logic state of the test point.

The second bridging experiment yielded similar results. The test sequence applied in the second experiment sensitized a path through both contact sites of a feedback bridging defect. The defect caused a significant delay in signal propagation along this path but did not cause a logic error. We reduced the frequency of the applied input stimulus to 1 MHz for this experiment. This allowed us to examine the transients generated as a single edge was propagated through the circuit under quiescent initial conditions, similar to the conditions of an impulse experiment. The

Magnitude and Phase SWs of the non-sensitized test points closest to the defect site showed variation over the entire range of frequencies analyzed. Moreover, the slower input stimulus enhanced the variations that occurred between the defective and non-defective devices in the time domain.

The open drain experiments provide further supporting evidence that defects cause regional signal variation that is best measured as phase shifts in the phase SWs. The open drains were introduced into 4-input NAND gates by removing Metal 1 between the p-transistor drain pairs. The test sequence for the first open drain experiment caused logic signal transitions to occur on all but one of the test points. Variations caused by process tolerances were measureable as changes in propagation delay in both the defect-free and defective device time domain SWs. However, the regional signal variation caused by the defect created distinct phase shifts at each of the test points that permitted the defective devices to be easily identified. Moreover, we observed a definite correlation between the change in propagation delay and the length of the sensitized path across the test points of each device in both open drain experiments. The correlation of multiple test point signals can be used to identify the global variation caused by process tolerances and reduce the number of false positive and fault negative defect detections.

5.0 Summary and Conclusions

We presented a new parametric testing method for digital integrated circuits called Transient Signal Analysis. In TSA, the transient signals of a device measured at multiple test points are used to detect defects. We introduced Signature Waveforms as a means of capturing signal differences between devices.

We used hardware experiments to demonstrate that defect detection was possible using the signals at test points that were not on logic signal propagation paths from the defect site. Similar to the stated advantages of I_{DDQ}, the ability to detect defects without requiring their faults to be propagated to observation points may reduce test set size and complexity. We also showed that it was possible to distinguish between the variations caused by defects and those caused by process tolerances by correlating the Signature Waveforms measured at distinct topological locations on the device. This attribute improves the accuracy of the test by reducing the number of false positive and false negative defect detections.

We introduced bridging and open drain defects into multiple versions of the ISCAS85 c432 circuit specification. The Signature Waveforms of four hardware experiments were analyzed in both the time and frequency domain. We demonstrated that the phase SWs were more useful than the time and magnitude SWs in providing a means of discriminating between the defect-free and defective devices. We observed distinct phase shifts in the SWs of both bridging and open drain defective devices and no significant phase variation in the SWs of the defect-free devices. Moreover, the procimity of the test point to the defect site and its output state determined the frequency components that were affected. Both of these effects supported our expectation that the defect causes regional signal variations in the defective device.

The global effects of process tolerances were best illustrated in the magnitude SWs of non-sensitized test points and in the time domain SWs of sensitized test points. We observed similar variations in the magnitude SWs of defect-free devices across all test points. We also noted a definite correlation between the amount of variation due to changes in propagation delay and the length of the sensitized path in the time domain SWs of defect-free devices. Both of these effects supported our expectation that process tolerance effects cause global signal variations that are proportional in all test point signals.

We are currently conducting a set of modeling experiments in order to characterize each of the coupling mechanisms, namely, the power supply, internodal, well and substrate. Based on the c432 experiments, we expect that the power supply is the predominant signal coupling mechanism and that measuring voltage transients directly on the supply rails would both increase the sensitivity of the test and reduce the number of test points required. The information obtained from the modeling experiments will help us determine the number and position of the test points and subsequently, the number and type of test vectors necessary to achieve a given fault coverage and quality level improvement factor. The detection capability of the method to other types of catastrophic and parametric defects is also under investigation as well as a statistical methodology based on cross correlation that will automatically distinguish between variations caused by process tolerances and those cause by defects.

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