Sensitivity Analysis of Quiescent Signal Analysis for Defect Detection

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Abstract

I_{DDQ} or steady state current testing has been extensively used in the industry as a mainstream defect detection and reliability screen. However, leakage current continues to increase significantly with each technology generation, making it difficult to use single threshold I_{DDQ} testing to differentiate between defective and defect-free chips. Alternative techniques that improve the resolution of I_{DDQ} testing have been proposed to replace the single threshold detection scheme. All of these techniques use a single I_{DDQ} measurement per circuit configuration for detection and thus the scalability of these techniques is limited. Quiescent Signal Analysis (QSA) is a novel I_{DDQ} defect detection and diagnosis technique that uses I_{DDQ} measurements at multiple chip supply pads. The use of multiple measurements points per chip naturally scales down of leakage and can significantly improve detection of subtle defects. In this paper, regression and ellipse analysis of the data collected from a test chip fabricated in a 65 nm process demonstrate the defect detection capabilities and limits of this technique.

1.0 Introduction

Background leakage current continues to increase as silicon technology moves forward. This trend reduces the effectiveness of I_{DDQ} testing methods as traditionally applied and is posing a challenge for newer alternative strategies [1]. Alternative methods rely on a self-relative or differential analysis, in which the average I_{DDQ} of each chip is factored into the pass/fail threshold. Although the application of these techniques to low power chips will continue, these methods are expected to become increasingly less effective for high performance ASICs with high background leakage currents.

An alternate strategy that may have better scaling properties is to distribute the total leakage current across a set of simultaneous measurements. This is accomplished by measuring the individual power supply port currents. Our method called Quiescent Signal Analysis (QSA) is designed to exploit this type of leakage calibration as a means of increasing defect detection resolution. A secondary diagnostic benefit of such a technique is described in [2-5].

In previous works, we developed several statistical based methods for processing the data collected from the simultaneous measurements. A linear regression analysis procedure was developed and applied to simulation data obtained from a commercial power grid in [6]. A hyperbola based method is described in [7] that performs defect detection using transient signal measurements. These techniques analyze multiple simultaneous measurements to accomplish three goals: 1) to detect the regional signal variation introduced by defects, 2) to scale down the magnitude of the chip's total current in the individual measurements and 3) to diminish or attenuate process induced signal variations. The latter includes both local (within die) and global (between die) variations in leakage current.

In this work, we apply linear regression analysis and a new technique called ellipse analysis to the data collected from a set of test chips. The test chips are fabricated in a 65 nm, 10 metal layer technology. The test chips incorporate an array of test structures that allow the insertion of a defect in any one of 4,000 locations. The design permits control over the magnitude of the defect current and leakage current. The results of our analysis confirm the regional nature of defect signal variations and demonstrate that detection sensitivity is strongly correlated with the position and magnitude of the defect current as well as the magnitude of the leakage current.

2.0 Related Work

The single-threshold I_{DDQ} technique relied on the fact that the steady state current distribution of defect-free chips is distinct from that of the defective ones. A chip that draws current that exceeds the defect-free current distribution by a fixed threshold is deemed as defective. With the advent of deep sub-micron technologies, the overlap in these distributions makes it difficult to set an absolute pass/fail threshold. The increase in sub-threshold and gate leakage currents in newer technologies can result in defect-free leakage currents that are significantly higher than the defect current. Thus, calibration methods are required to reduce the adverse effects of high leakage currents on defect current resolution. Several techniques based on a self-relative or differential analysis are proposed as a solution to this problem. A current signature method is proposed by Gattiker et. al. [8], that looks for discontinuities in the curve obtained by sorting I_{DDQ} measurements in ascending order. Delta I_{DDQ} is a differential I_{DDQ} method proposed by Thibeault [9] in which differences between successive I_{DDQ}

measurements are compared to a threshold. Maxwell et. al. [10], proposed a current ratio method where chip specific thresholds are derived by using vectors that produce the minimum and maximum I_{DDQ} values. A clustering technique that groups good chips separately from bad chips is proposed by Jandhyala et. al. [11]. Daasch et. al. [12] describe a method that predicts device I_{DDQ} using the spatial proximity correlations among chips on a wafer. Variyam [13] proposes a linear prediction based technique in which each I_{DDQ} value among a set of values for a given chip is predicted from the remaining I_{DDQ} values in the set. Singh et. al [14] showed that I_{DDQ} readings of the neighboring die on a wafer can be used for variance reduction and to identify wafer-level spatial outliers. Sabade et. al [15][16] have also developed methods based on wafer-level spatial correlation analysis in which they derive a maximum defect-free I_{DDQ} threshold from the analysis of neighboring die.

Many of these process-tolerant I_{DDQ} methods use relative pass/fail thresholds instead of absolute thresholds. Also the other major similarity of these techniques is that they use a single I_{DDQ} measurement per circuit configuration per die. As the variance in the I_{DDQ} values increases, it tends to increase the threshold bands in most of these techniques, thus decreasing their defect resolution. QSA differs from these methods by correlating individual supply I_{DDQ}s within each state vector. Statistical characterization of the defect-free chips in combination with outlier analysis is used to differentiate defect-free and defective devices. Therefore, the cross-correlation performed in QSA additionally calibrates for vector-to-vector variations. This is likely to further improve the process tolerance of the method. It is also noted that QSA can be used in combination with any of the existing vector-to-vector analysis techniques to further improve defect resolution.

Another advantage of QSA is the natural scalability that this type of approach incorporates. The scalability features of QSA should make it possible for it to remain effective at detecting defects as chips get larger and incorporate larger numbers of more densely packed transistors. QSA is designed to exploit design trends that add additional supply ports (pads that interface to the external supply) as chip sizes and current requirements increase. However, it should be noted that this benefit of increased resolution comes with the cost of increased test time as multiple measurements need to be performed per vector.

Perhaps a greater benefit of using multiple power supply signals is that they offer information beyond defect detection. In our previous work, we have demonstrated the ability of QSA for application to defect diagnosis [2-5]. The procedure predicts the (x,y) coordinates at which a defect draws current from the power grid in the layout. To our knowledge, no other method that is based on the analysis of a chip's electrical signals is able to provide this type of information. Such information is extremely useful in failure analysis procedures, which are designed to determine the root cause of chip failures.

3.0 Test Chip Design

A block diagram of the test chip design is shown in Figure 1(a). It consists of a 80x50 array of calibration circuits (CCs) shown in Figure 1(b). Each CC consists of three FFs connected in a scan chain configuration, a parallel set of shorting inverters, and a *defect enable transistor* connected to a globally routed *defect emulation wire.* Two power grids are interleaved over this array, one connected to the FFs and the second connected to the shorting inverters and defect enable transistors. The V_{DD} tap points shown in Figure 1(a) as V_{00}, V_{01}, V_{10} and V_{11} connect to the second power grid and wire out of the chip through separate pins. The array is 558 μm in width and 377 μm in height.

The connection of the shorting inverters and the defect enable transistors to point sources on the power grid allow for a power-ground short or a connection between the power grid and defect emulation wire, respectively. Each of these is controlled by the FFs. For example, FF_1 in Figure 1(b) is used to control the defect enable transistor, which enables a connection between the power grid and the defect emulation wire. In this way, a defect can be emulated at any point in the array by driving the defect emulation wire with a voltage source, labeled *defect source* in Figure 1(b), and scanning the appropriate bit pattern into the scan chain. The voltage set into the defect source controls the magnitude of the shorting current, where lower voltages (below 0.9 V) introduce more significant currents. Lower voltages also increase the leakage current through the off p-channel transistors at other positions in the array (which adds to the leakage current already present in the shorting inverters). Therefore, it is possible to analyze a variety of shorting and leakage current configurations by controlling the connection position and voltage on the defect emulation wire.

FF_2 and FF_3 control the gates of the shorting inverters. A power-ground short is introduced by scanning a 1-0 bit pattern into the two FFs, respectively. Individual control of each transistor in the inverters also permits alternative leakage distributions to be configured in the array by scanning in a pattern that leaves one or both of the transistors in the off state (using one of the three remaining bit patterns, 0-0, 1-0 or 1-1).

4.0 Test Chip Experiments

Two sets of experiments were conducted on three copies of the test chip. In both sets, individual currents were measured at each of the four V_{DD} tap points. The first set made use of the shorting inverters (the defect emulation wire was disconnected). Here, the scan chain was configured to cause one of the CC shorting inverters to short and the four currents at each V_{DD} tap point were measured.
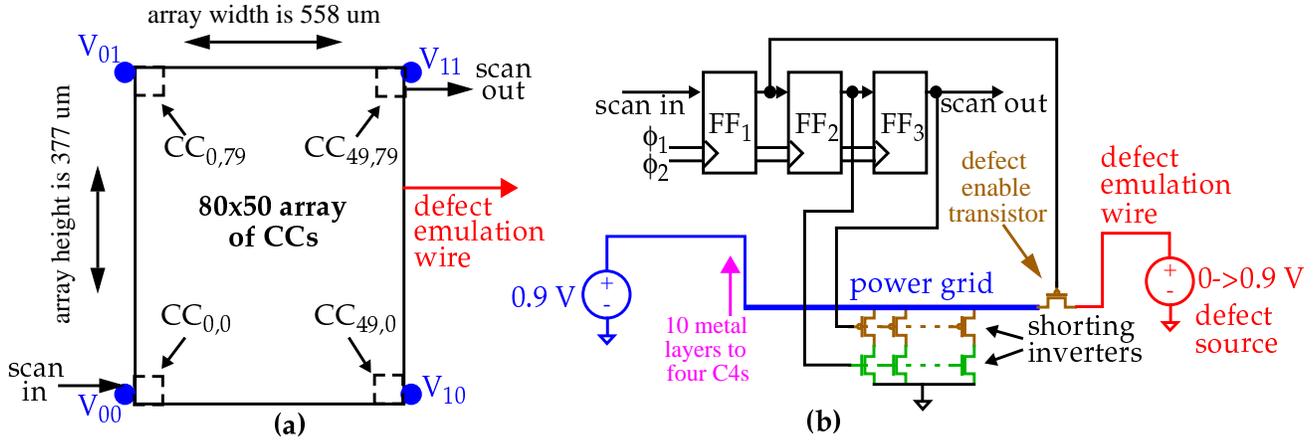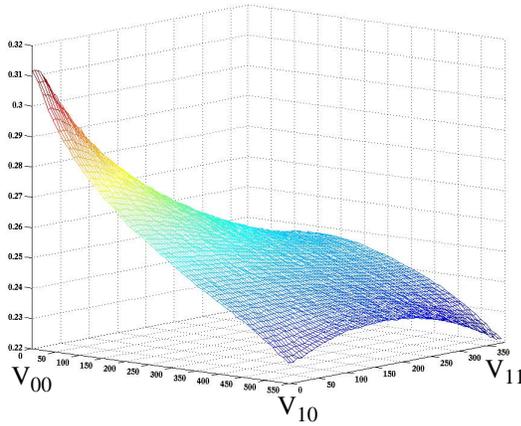
Figure 1. (a) Test CUT of CCs, (b) CC circuit.

Figure 2. V_{00} **normalized current profile.**

This experiment was repeated 4,000 times, once for each CC in the array.

The current profile for V_{00} is shown in Figure 2. Here, the x & y axis represent the (x,y) space of the CC array given in microns. The z axis represents the normalized shorting currents (leakage is subtracted) measured in V_{00} as each of the 4,000 CCs are individually enabled. The V_{00} currents are normalized by dividing the measured value by the sum of the currents at all V_{DD} tap points. The z values are largest near V_{00} because CCs near this location draw a larger fraction of their current (approximately 31%) from V_{00} than CCs that are further removed. The other extreme, i.e., the smallest values of z, occur at locations near the remaining three V_{DD} tap points. The smooth monotonically decreasing nature of the curve from largest to smallest clearly shows the regional behavior induced by the power grid resistance characteristics.

The data points of interest from this analysis are those current values associated with the CCs near the V_{DD} tap points. Figure 1(a) identifies four CC circuits, $CC_{0,0}$, $CC_{0,79}$, $CC_{49,0}$ and $CC_{49,79}$ positioned underneath the V_{DD} tap points. The currents measured with these four CCs enabled one at a time can be used to calibrate for resistance variations in the connections from the external power supply source to the V_{DD} tap points. Differences in these resistances across chips adversely affects our defect detection techniques. The calibration procedure that we developed is described in [17].

The second set of experiments involve the use of the defect emulation wire (the shorting inverters are disabled). A set of 100 locations in the array was randomly selected and represent the CCs under investigation in these experiments. The currents through the four V_{DD} tap points were measured for each of the 100 experiments under 19 different values of the defect source voltage. Therefore, for each chip, 1,900 experiments were conducted.

In each experiment, the currents were measured under two state configurations. The first state configuration allowed leakage current to be measured with the defect source set to a specific value. In this case, all defect enable transistors were turned off. The second state configuration enabled the defect enable transistor. This caused a short between the power grid and defect emulation wire at a specific point in the array. The currents measured under this configuration include a component introduced by the emulated defect.

Table 1 specifies the voltage drop between the defect source and power grid in the first column and the average value of the ratio of defect current to leakage current in the remaining columns for each of the three chips. The numerator in the ratio is computed by subtracting the leakage current through the defect source with defect enable transistors off from the value measured when one of the defect enable transistors is turned on. The denominator is computed from the sum of the V_{DD} tap point leakages (with defect enable transistors turned off). Since there are 100 defect sites, the

average is computed over 100 measurements for each chip (columns) and each voltage drop (rows).

V_{drop} (V)	C1 I_{norm} (ratio)	C2 I_{norm} (ratio)	C3 I_{norm} (ratio)
0.05	0.16	0.12	0.88
0.10	0.29	0.22	1.61
0.15	0.41	0.31	2.23
0.20	0.51	0.39	2.73
0.25	0.58	0.43	3.09
0.30	0.63	0.47	3.36
0.35	0.67	0.49	3.42
0.40	0.69	0.50	3.54
0.45	0.74	0.56	3.56
0.50	0.69	0.50	3.38
0.55	0.67	0.48	3.16
0.60	0.64	0.46	2.94
0.65	0.60	0.42	2.61
0.70	0.67	0.51	2.45
0.75	0.50	0.35	2.00
0.80	0.45	0.31	1.72
0.85	0.39	0.27	1.47
0.90	0.34	0.24	1.25

Table 1: Normalized defect currents.

The ratio expresses the relative magnitude of total defect current to leakage, and is the basis of our sensitivity analysis. For example, the range of the ratios changes by over an order of magnitude from 0.12 (hard to detect) to 3.38 (easier to detect). The ratios for C1 and C2 are lower than those for C3 because C3 is a "low leakage" chip. The smaller value of leakage in the denominator creates larger ratios for this chip. Also notable is the trend in the ratios for any given chip across the V_{drop} values. For example, the largest ratios for all three chips occur with V_{drop} at 0.45 volts. The ratios then begin to *decrease* for larger voltage drops. This occurs because the defect enable transistor begins to saturate at 0.45 volts, and therefore, the numerator does not increase much beyond this voltage drop. The leakage current, on the other hand, continues to increase for larger voltage drops, and this causes the ratio to get smaller.

5.0 Detection Procedures

The data used as input to the statistical procedures is first calibrated for *probing* resistance variations using a procedure described in previous work [17]. Due to space limitations, the probe card calibration procedure is not discussed in this paper. We also describe and demonstrate a statistical defect detection procedure based on linear regression analysis in previous works [6]. The features of that procedure as well as a new statistical procedure, called ellipse analysis, are outlined in this section.
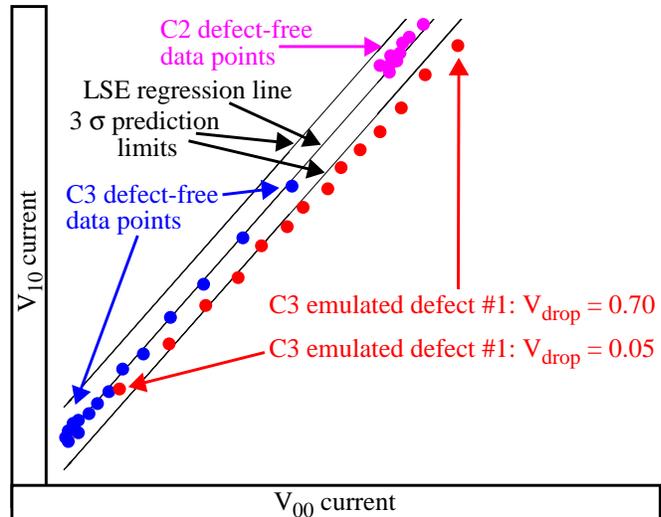

Figure 3. V_{00}-V_{01} regression analysis.

5.1 Linear Regression Analysis

The chip-to-chip variation in I_{DDQ} is well characterized using a regression model which analyzes the measured currents from pairings of V_{DD} tap points. Regressing the values from one V_{DD} tap point to those measured at another V_{DD} tap point produces a near linear relationship across chips. Figure 3 plots a set of the measured I_{DDQs} for V_{DD} tap point pairing V_{00} (x-axis) and V_{10} (y-axis). The data points labeled *defect-free* were collected with the defect enable transistors turned off. For example, the data points labeled *C3 defect-free data points* represent the I_{DDQs} measured at these two V_{DD} tap points on chip C3, each under a different V_{drop} values, as listed row-wise in Table 1. The same is true for the points labeled *C2 defect-free data points* (note, only the lower left region of the scatter plot is shown). The line labeled *LSE regression line* represents a least squares estimate of the regression line through the 57 defect-free data points in the scatter plot. The parabolic curves labeled *3 σ prediction limits* represent the threshold between the defect-free space and the defective space.

The points labeled *C3 emulated defect #1* represent the I_{DDQs} when measured with one of the defect enable transistors turned on. The 3 data points in the lower left portion of the scatter plot are associated with $V_{drop}s$ of 0.05, 0.10 and 0.15 V. They are within the prediction limits and therefore are not detected for this V_{DD} tap point pairing. Positive detections, however, do occur for the other (larger) values of V_{drop} since the data points are positioned outside the prediction limits.

5.2 Ellipse Analysis

The ellipse analysis procedure that we use is similar to the linear regression analysis procedure. In both cases, the I_{DDQs} from adjacent V_{DD} tap points are plotted in 2 dimen-
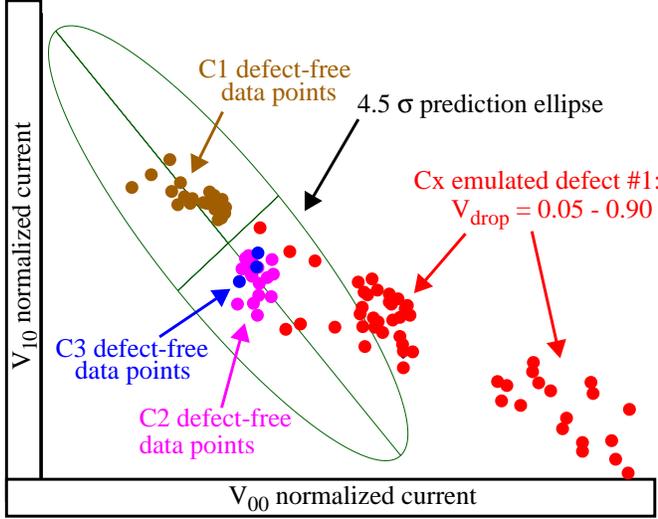
Figure 4. V_{00}-V_{01} ellipse analysis.

sional scatter plots. However, for ellipse analysis, the I_{DDQ}s are first *normalized* by dividing each value by the sum of the I_{DDQ}s measured at the four V_{DD} tap points. This operation significantly reduces the effects of non-regional process variations across the chips and effectively compresses the data points distributed along the regression line in Figure 3 into a cluster.

Figure 4 shows the cluster that results for V_{DD} tap points, V_{00} and V_{10} across the three chips. Also shown is a 4.5 σ prediction ellipse generated from the eigen values of the covariance matrix and X^2 (chi-square) distribution statistic. Equation 1 gives the formula for the length of the principle axis, *a*, for the ellipse, given eigen value λ_0 and the value of the X^2 statistic of second degree evaluated at 0.99999 (4.5 σ). The *b* axis is defined in a similar

$$a = sqrt(23.026 \times \lambda_0) \qquad (1)$$

fashion. The eigen vectors define the orientation of the ellipse in 2 dimensional space.

The prediction ellipse defines the limits in which defect-free chips are expected to generate data points. The data points labeled *Cx emulated defect #1: V_{drop} = 0.05 - 0.90* are produced under the tests that enable the defect enable transistor in chip x = 1, 2 and 3. Some of these data points appear inside the ellipse and therefore are classified under this V_{DD} tap point pairing as belonging to a defect-free chip. Similar to the regression analysis case discussed in relation to Figure 3, these data points are associated with small values of V_{drop}. Conversely, positive defect detection decisions occur for the data points positioned outside the ellipse.

5.3 Details of the Statistical Analysis Procedure

The defect detection procedures are formulated on the

analysis of scatter plots, such as those shown in Figures 3 and 4. Four scatter plots were analyzed for each defect and V_{drop} value, one for each adjacent pairing of V_{DD} tap points shown in Figure 1. A defect is counted as detected if one or more of its data points falls outside the prediction limits (for regression analysis) or the prediction ellipse (for ellipse analysis).

As indicated, 100 emulated defect position were chosen at random among the set of 4,000 within the array. For each defect, 18 tests were performed, each using a different V_{drop} value. Therefore, 1,800 emulated defects were evaluated for each chip, yielding a total of 5,400 emulated defects (3 chips * 1,800 emulated defects/chip).

The statistical limits were set such that all defect-free points fell within the limits. This required a 3 σ limit for regression analysis and 4.5 σ for ellipse analysis. These limits are different because the division operation performed for ellipse analysis amplifies the measurement noise in the data, causing the defect-free points to be more widely distributed. The effect is particularly evident for the low leakage chip C3, where our signal-to-noise ratio is smallest. On-going work is refining our measurement apparatus in hopes of raising the signal-to-noise ratio by an order of magnitude. Under the present setup, it was necessary to both widen the limits under the ellipse analysis procedure to 4.5 σ and remove defect-free values below a certain absolute current threshold. This is evident in Figure 4 which shows only 3 of the 19 defect-free data points for chip C3. In contrast, all 19*3= 57 defect-free data points were used in regression analysis. A lesson learned from these experiments is that regression analysis is more robust to measurement noise.

The standard statistical method of analyzing *deviation from the mean* in scatter plots is through *residuals*. A residual is defined to be the shortest distance from a data point to the regression line, for regression analysis, and to the center of the ellipse, for ellipse analysis. This distance is usually converted into a standardized residual using Equation 2.

$$ZRES = \frac{residual}{\sqrt{MSE}} \qquad (2)$$

Here, *MSE* represents the *mean square error* or the variance of the defect-free data points from their respective means. For regression, the mean for a particular value of x is the regression line y value. For ellipse analysis, the mean is the (x,y) center of the ellipse.

In this paper, we report two quantities that reflect the detection sensitivity of these statistical procedures. The first is the number of detections for each defect (maximum value is 4) and the second is the maximum standardized residual (ZRES). For missed detections in which the data points for the emulated defect fell within the limits in all 4 scatter plots, the number of detections and the maximum
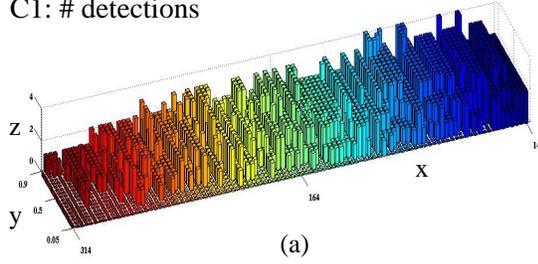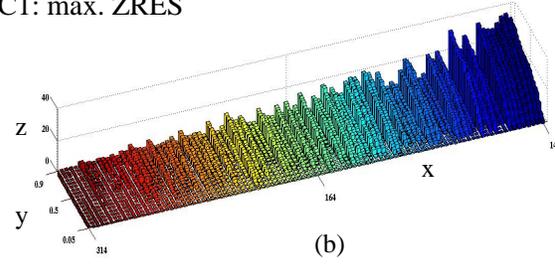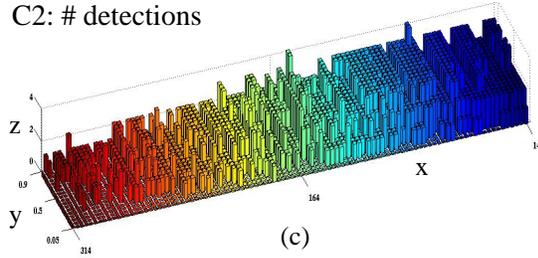
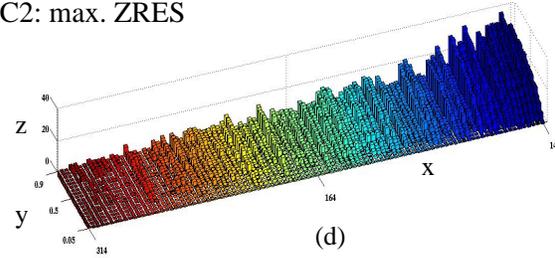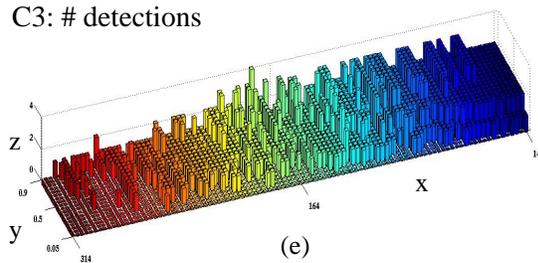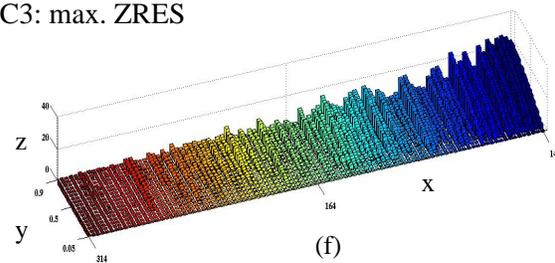**Figure 5. Regression Analysis Histogram Results**

ZRES are both given as 0. Both of these metrics convey the level of confidence present in a positive detection decision, with higher numbers yielding higher confidence.

6.0 Experimental Results

6.1 Regression Analysis

The results of applying regression analysis to the data are shown in a series of histograms in Figure 5. Each histogram displays the results of the number of detections (left) or the maximum ZRES (right) for each of the three chips (rows). As indicated above, an emulated defect is considered detected when the number of detections and the maximum ZRES are greater than 0.

The data within each histogram is organized as follows. The x axis represents the emulated defects where the defects are labeled according to their distance to the nearest V_{DD} tap point. The y axis represents the V_{drop} value between the power grid and defect emulation wire. The z axis represents either the number of detections or maximum ZRES value. Therefore, each histogram has 100 elements along the x axis and 18 elements along the y axis, for a total of 1,800 emulated defects per chip.

The most noticeable trend in the histograms is the gradual reduction of the values from right to left along the x

axis. As indicated above, the defects are ordered in the histogram according to their distance to a V_{DD} tap point. The elements on the far right in the histogram have the smallest values and therefore are closest to a V_{DD} tap point. This trend clearly indicates that better detection sensitivity is obtained for defects closer to the measurement points. This is true because the resistance characteristics of the power grid enhance the *regional disturbance* introduced by the defect at points closer to the V_{DD} tap points. This holds true independent of the ratio of defect current to leakage current, that is conveyed in the V_{drop} value plotted along the y axis.

Most of the missed detections occur in the left portion of the histograms. The emulated defects in these cases are near the center of the power grid. We call this region the *resistive middle*. Emulated defects in this region are difficult to distinguish from process variation effects because the defect current distributes with more uniformly to the 4 V_{DD} tap points. It is important to note that the *resistive middle* holds true only with respect to the neighboring V_{DD} tap points. Most commercial grids have more than 4 supply ports and therefore, it is likely that many of the missed detections in this analysis will be detected by the other V_{DD}
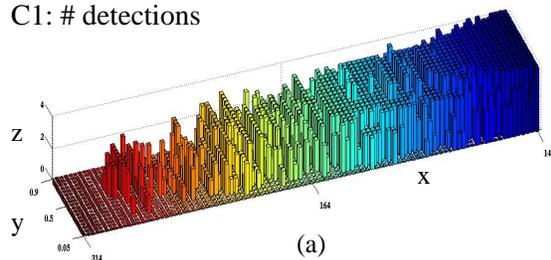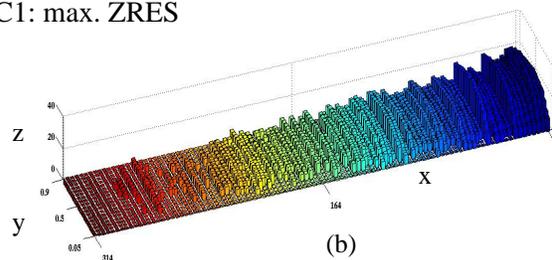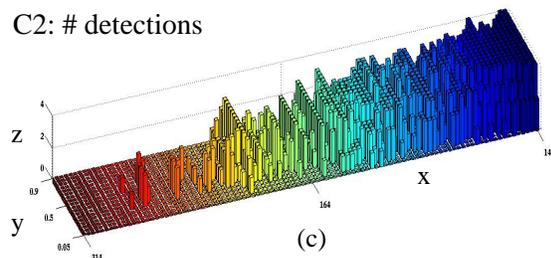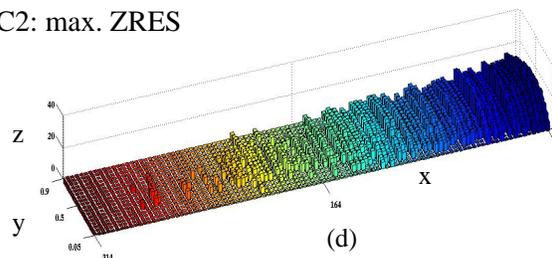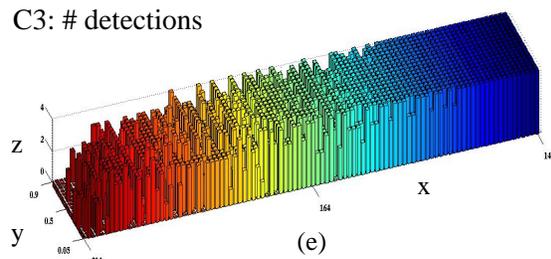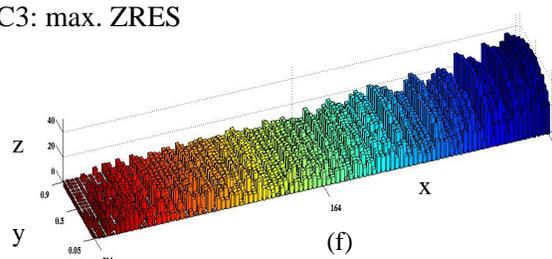
Figure 6. Ellipse Analysis Histogram Results

tap point pairings outside this *quad*. The design of this chip actually includes two additional V_{DD} tap points located midway between the vertical pairs, V_{00}-V_{01} and V_{10}-V_{11}. We will report the results of a *two quad* (6 V_{DD} tap points) analysis in a future work to verify this hypothesis (which is validated in previous work through simulation experiments).

The second, somewhat less evident, trend in the histogram data is the near monotonic nature of the data along the *y* axis. This is particularly evident in the maximum ZRES histograms in which the largest values occur for the V_{drop} *y* slice associated with 0.90. The ratios given in Table 1 indicate that the easiest detections should occur along the *y* slice associated with 0.45 V_{drop}. It is here that the ratio of defect current to leakage current is largest. However, this expected parabolic trend is not evident in the histograms.

6.2 Ellipse Analysis

The ellipse analysis results are shown by the histograms in Figure 6. The format of these histograms is identical to those given in Figure 5 for ease of comparison. The trend along the *x* axis described above for regression analysis also holds true here. The most notable difference is in

the *# detection* histograms shown for C2 and C3, i.e., Figures 6(c) and (e). Unlike the regression analysis results, which portray a stronger degree of uniformity with regard to defect detections across all three chips, the ellipse analysis results for chip C2 show a larger number of misses relative to C1 while chip C3 shows fewer numbers of misses. As indicated in Section 5.3, the differences in leakage currents among the chips and the existing signal-to-noise ratio of the instrumentation setup combine to create anomalies that are more evident here because of the normalization operation.

In contrast to the regression analysis data, the trend along the *y* axis, particularly in the maximum ZRES histograms, is parabolic in shape. This trend correlates well with the ratios given in Table 1. The peak values in the maximum ZRES histograms appear to occur toward the center, i.e., for the *y* slice associated with V_{drop} of 0.45 V. The numerical analysis given in the next section confirms this visually-derived conclusion.

6.3 Summary

Table 2 summarizes the number of emulated defects that were detected in the three chips for both analysis, broken down by V_{drop}. The maximum value for each entry is

300 (100 emulated defects * 3 chips). The total number of detections (sum of the two columns) is 4020 and 3775 for regression and ellipse analysis respectively. This indicates that regression is only slightly superior to ellipse analysis with regard to detection capability. However, the distributions are significantly different. For example, regression is able to detect only 28 of the emulated defects with small defect currents while the ellipse analysis does fairly well at 116 detections. On the other hand, regression is clearly superior for higher defect and leakage current combinations (bottom of the table). For example, at V_{drop} at 0.90 V, regression detects 285 of the emulated defects while ellipse analysis detects only 180. The monotonic verses parabolic nature of the maximum ZRES curves referenced in the preceding sections is reflected in these tabulated values.

V_{drop}	Regression	Ellipse
0.05	28	116
0.10	95	156
0.15	150	195
0.20	188	210
0.25	211	225
0.30	227	227
0.35	236	241
0.40	240	232
0.45	245	234
0.50	255	238
0.55	255	234
0.60	262	232
0.65	260	232
0.70	270	219
0.75	265	210
0.80	277	201
0.85	271	193
0.90	285	180
Total of 5400	4020	3775

Table 2: Number of defects detected

7.0 Conclusions

The defect sensitivity of Quiescent Signal Analysis is investigated in this paper. The data from three test chips fabricated in a 65 nm, 10 metal layer technology are analyzed using two statistical methods, one based on regression analysis and one based on ellipse analysis. The experimental design permits defects to be emulated in a 4,000 element array of test circuits. External control of both the emulated defect current and leakage current is provided through a globally routed defect emulation wire and external power source. The results of analyzing the data from 100 emulated defects indicates that the application of our simulation derived methods are capable of detecting approximately 70% of the emulated defects over a wide range of defect and leakage current combinations.

9.0 References

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