Multiple Supply Pad I_{DDQ}-based Defect Detection Techniques Applied to Hardware Test Chips

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Abstract

The large magnitude of background leakage currents in current technologies continues to reduce the effectiveness of conventional I_{DDQ} testing methods. Newer methods improve defect resolution using self-relative calibration techniques or correlation analysis of nearest neighbor data. Our techniques, which correlate multiple supply pad I_{DDQ}s from the same chip, represent the limit in what is achievable using self-relative and correlation analysis of data collected "in the neighborhood". However, the collection and analysis of multiple I_{DDQ}s from the same chip introduces new challenges not yet encountered in the I_{DDQ} testing. Many of these new problems are eloquently solved using a simple on-chip calibration circuit. Defect detection techniques and calibration methods designed to deal with, e.g., variations in probe card contact resistance, were developed in previous work using simulation experiments. In this paper, these simulation derived methods are verified in hardware chips fabricated in a 65 nm process. The data from 12 test chips is analyzed to determine the defect detection capabilities and limitations of our techniques.

1.0 Introduction

Background leakage current continues to increase as silicon technology moves forward. This trend reduces the effectiveness of I_{DDQ} testing methods as traditionally practiced and is posing a challenge for newer alternative strategies [1]. Alternative methods rely on a self-relative or differential analysis, in which the average I_{DDQ} of each chip is factored into the pass/fail threshold. Although the application of these techniques to low power chips will continue, these methods are expected to become increasingly less effective for high performance ASICs with high background leakage currents.

An alternate strategy that may have better scaling properties is to distribute the total leakage current across a set of simultaneous measurements. This is accomplished by measuring the individual power port currents. Our method called Quiescent Signal Analysis (QSA) is designed to exploit this type of measurement scheme as a means of increasing the ratio of defect current to leakage current. A secondary diagnostic benefit of such a technique is described in [2-5].

In previous works, we developed several statistical based methods for processing the data collected from the simultaneous measurements. A linear regression analysis procedure was developed and applied to simulation data obtained from a commercial power grid in [6]. A hyperbola based method is described in [7] that performs defect detection using transient signal measurements. These techniques analyze multiple simultaneous measurements to accomplish three goals: 1) to detect the local signal variations introduced by defects at point sources in the layout, 2) to reduce the adverse impact of background leakage current and 3) to diminish the adverse effects of within-die and between-die process variations.

In this work, we apply linear regression analysis and ellipse analysis to the data collected from a set of 12 test chips. The test chips are fabricated in a 65 nm, 10 metal layer technology. The test chips incorporate an array of test structures that allow a defect to be emulated in one or more of 4,000 distinct locations on the chip. The design permits control over the magnitude of the emulated defect current and leakage current. The results of our analysis confirm the localized nature of defect signal variations and demonstrate that detection sensitivity is strongly correlated with the position and magnitude of the defect current as well as the magnitude of the leakage current.

2.0 Background

The single-threshold I_{DDQ} technique relied on the fact that the steady state current distribution of defect-free chips is distinct from that of the defective chips. A chip that draws current that exceeds the defect-free current distribution by a fixed threshold is deemed defective. In deep sub-micron technologies, however, the distributions overlap, and it is not possible to set an absolute pass/fail threshold that distinguishes defect-free and defective chips. The increase in subthreshold and gate leakage currents in newer technologies can result in background leakage currents that are significantly higher than the defect current. Thus, alternative techniques are needed to reduce the adverse effects of high background leakage currents on defect current resolution.

Several techniques based on a self-relative or differential analysis are proposed as a solution to this problem. A current signature method is proposed by Gattiker et al. [8], that looks for discontinuities in the curve obtained by sort-

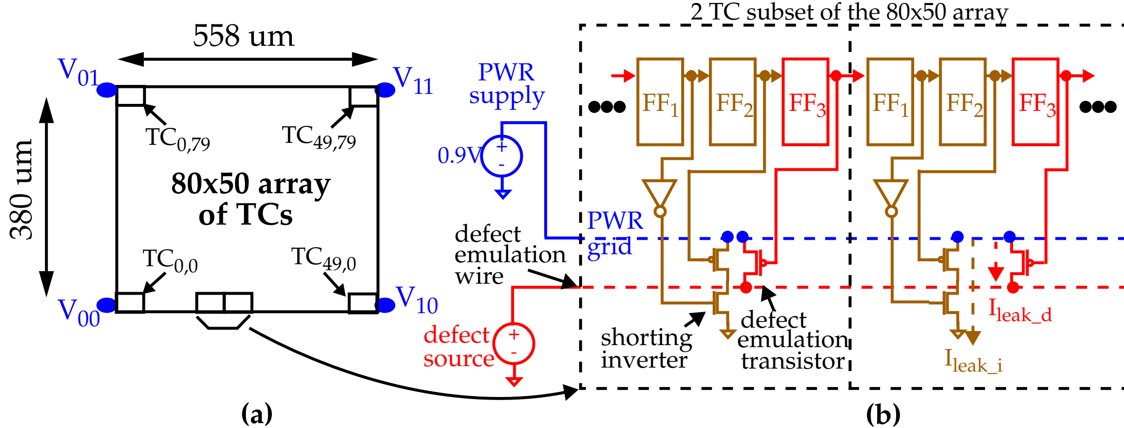

Figure 1. (a) Block diagram of the test structure and (b) details of the test cells (TC).

ing I_{DDQ} measurements in ascending order. Delta I_{DDQ} is a differential I_{DDQ} method proposed by Thibeault [9] in which differences between successive I_{DDQ} measurements are compared to a threshold. Maxwell et al. [10], proposed a current ratio method where chip specific thresholds are derived by using vectors that produce the minimum and maximum I_{DDQ} values. A clustering technique that groups good chips separately from bad chips is proposed by Jandhyala et al. [11]. Daasch et al. [12] describe a method that predicts device I_{DDQ} using the spatial proximity correlations among chips on a wafer. Variyam [13] proposes a linear prediction based technique in which each I_{DDQ} value among a set of values for a given chip is predicted from the remaining I_{DDQ} values in the set. Singh et al. [14] showed that I_{DDQ} readings of the neighboring die on a wafer can be used for variance reduction and to identify wafer-level spatial outliers. Sabade et al. [15][16] have also developed methods based on wafer-level spatial correlation analysis in which they derive a maximum defect-free I_{DDQ} threshold from the analysis of neighboring die.

Many of these process-tolerant I_{DDQ} methods use relative pass/fail thresholds instead of absolute thresholds, and all are based on the use of *global*, i.e., chip-wide, I_{DDQ} measurements. As the variance in I_{DDQ} increases, it tends to increase the threshold bands in many of these techniques, thus decreasing their sensitivity to detect defects. QSA differs from these methods by cross-correlating *local*, i.e., within-chip, I_{DDQ} measurements obtained from the multiple, individual supply ports on the chip. In addition to the benefits identified in the Introduction, the local I_{DDQ} measurements eliminate the adverse effects of vector-to-vector variations inherent in global I_{DDQ} measurement strategies.

3.0 Test Chip Design

A block diagram of the test chip design is shown in Figure 1(a). It consists of a 80x50 array of test circuits (TCs) that occupies an area of dimension 558 µm in width and 380 µm in height. Each TC consists of three FFs connected in a scan chain configuration, a *shorting inverter*, and a *defect emulation transistor* connected to a globally routed *defect emulation wire*. A schematic diagram of two adjacent TCs is shown in Figure 2(b). The shorting inverters and defect emulation transistors within each TC connect to the same point on the power grid.

The connection of the shorting inverters and the defect emulation transistors to point sources on the power grid enable two types of shorts to be introduced within any one (or more) of the 4,000 TCs. The first type shorts the power grid to ground through the inverter using FF_1 and FF_2 and the second type shorts the power grid to the defect emulation wire using FF_3. For the first type, the magnitude of the shorting current is defined by the external power supply voltage, labeled *PWR supply* in Figure 1(b).[1] For the second type, the magnitude of the shorting current is controlled through an external voltage source, labeled *defect source*. Given this configuration, a defect can be emulated at any point in the array by setting the defect source to a value less than the PWR supply voltage and scanning a bit pattern into the scan chain such that exactly one FF_3 contains a 0 and the remaining 11,999 FFs contain 1's.

In addition to controlling the magnitude of the defect current, the defect source also influences the magnitude of the background leakage current, as measured through the PWR supply. The total leakage current can be decomposed into two types, shown as $I_{leak_i(nverter)}$ and $I_{leak_d(efect)}$ in the right-most TC of Figure 1(b). Given the defect emulation wire connects to the drains of 4,000 defect emulation transistors, only one of which is enabled in a particular experiment, the remaining 3,999 transistors will source

1. The PWR supply is held constant in our experiments at 0.9 V.

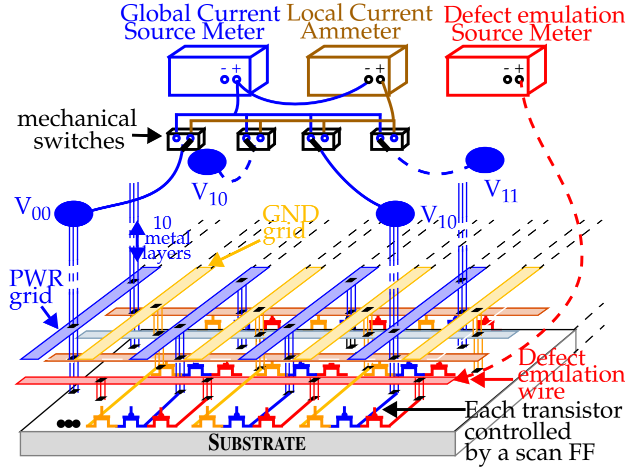

Figure 2. External Instrumentation Setup.

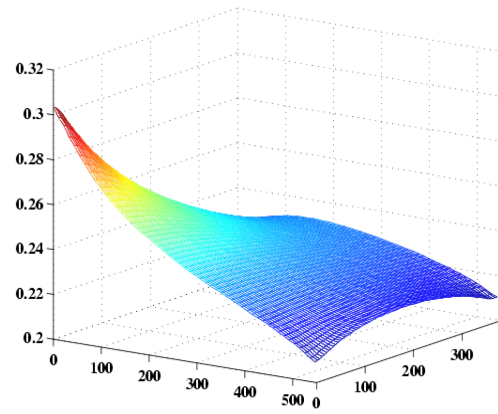

Figure 3. (a) I_{norm_00} profile.

leakage current from the PWR supply proportional to the magnitude of the defect source voltage. This leakage, I_{leak_d}, adds to the leakage current already present through the shorting inverters, I_{leak_i}. Therefore, it is possible to analyze a variety of shorting and leakage current configurations by controlling the states of the defect emulation transistors and voltage on the defect emulation wire.

The external instrumentation setup is shown in Figure 2. As indicated above, the power ports, labeled V_{00} through V_{11} wire out of the chip on separate pins in the package. The individual power pins are each wired to a low resistance mechanical switch as shown along the top portion in Figure 2. The switch can be configured in a left or right position. The left and right outputs across the switches connect to a common wire that routes to the *Global Current Source Meter* (GCSM) and *Local Current Ammeter* (LCA), respectively.

The GCSM is configured to provide 0.9 Volts to the PWR grid and is also able to measure current with accuracies less than 100 nA. The LCA is wired in series with the GCSM and allows the individual power port (*local*) currents, to be measured at the same level of accuracy. As an example, the configuration of the switches as shown in Figure 2 allow the local V_{00} current, I_{00}, as well as the global current to be measured. The *Defect Emulation Source Meter* (DESM) is used to set the voltage of and measure the current, I_{def}, through the defect emulation wire on a separate pin in the package (not shown).

4.0 Power Grid Characterization Experiments

The first set of experiments is designed to determine how the grid resistance influences the magnitude of the local currents. In these experiments, the defect emulation wire is disconnected and the defect emulation transistors are disabled. Instead, the shorting inverters are used to provide the stimulus to the grid.

In these experiments, each of the 4,000 shorting inverters from one of the chips is enabled, one at a time, and the global and local currents are measured. Given that we are interested in the characteristics of the grid resistance and its influence on the local current distributions from point sources in the layout, the following steps are also performed. After testing each element of the array, the shorting inverter of the TC under test is disabled and the global and local leakage currents are measured and subtracted from the values measured with the shorting inverter enabled. These *difference currents* are then *normalized* by dividing by the global current. This type of normalization virtually eliminates the variations in the transistor current magnitudes caused by process variations.

Figure 3 shows the current profile derived from the normalized local currents, I_{norm_00}. Here, the *x* and *y* axes represent the (*x*, *y*) plane of the TC array and I_{norm_00} is plotted on the *z* axis. The local currents are largest near V_{00} because TCs near this location draw a larger fraction of their current from V_{00} (maximum is approximately 31%) than TCs that are further removed. The degree to which the grid resistance influences the distribution of currents to the V_{DD}s is reflected in the range, which is approximately 11%. The smooth monotonically decreasing nature of the surface from largest to smallest provides the basis on which defect detection methodologies can be built, as described in the following sections.

5.0 I_{DDQ} Defect Detection Experiments

These experiments are designed to investigate our defect detection methodologies and the degree of sensitivity that they posses with regard to detecting defects that draw only small amounts of current. These objectives are better met through the use of the defect emulation transistors and corresponding defect emulation wire because both the position and magnitude of the emulated defect current

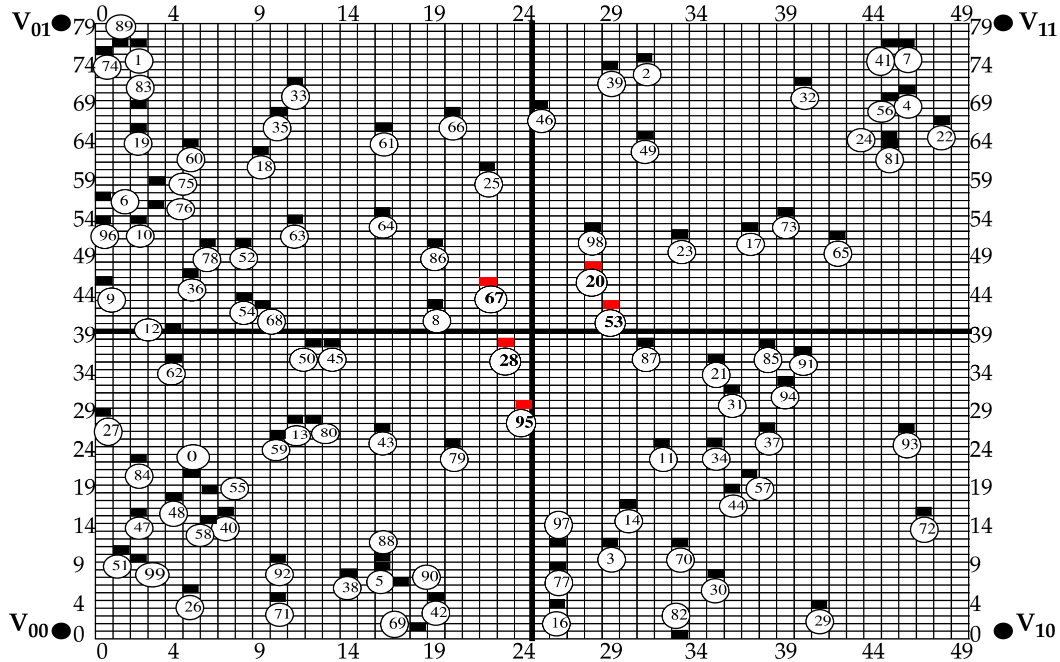

Figure 4. Positions of the 100 randomly selected TCs.

can be controlled.

5.1 Data Collection Procedure

Unlike the power grid characterization experiments which tested all 4,000 elements of the TC array, in these experiments, only a subset of 100 TCs are tested. The set of randomly selected TCs within the 80x50 array are shown in Figure 4. The numbered positions are the TCs under investigation in these experiments.

For each of the 12 chips, a series of measurements were made for each of the TCs under different voltage configurations of the DESM, i.e., the source meter that drives the defect emulation wire. The first experiment for each chip is referred to the *defect-free* experiment. In this experiment, the state of all scan chain FFs is set to 1, which disables both the shorting inverters and the defect emulation transistors within all TCs in the array. The DESM is then swept across a sequence of voltages, from 0.9 V to 0.0 V in 50 millivolt intervals, for a total of 19 steps. At each DESM voltage, a set of 4 local and 4 global currents are measured. The same sequence of operations is performed with each of the defect emulation transistors enabled, one at a time.

5.2 Data Sets and Pairings

For each chip, the data collection procedure produces 1,919 data sets. 19 of these data sets represent data from the defect-free experiments and 1900 (19 * 100 emulated defects) represent data from the emulated defect experiments. However, the emulated defect experiment with the DESM voltage set to 0.9 V is not meaningful because there

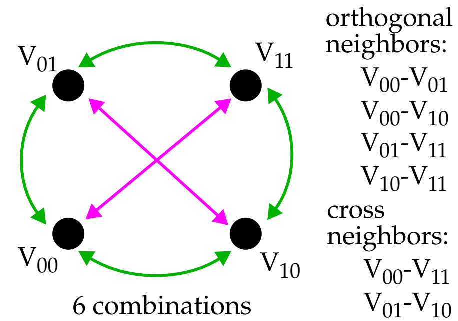

Figure 5. V_{DD} pairing combinations.

is no voltage drop across the defect emulation transistor. Therefore, only 18 of the 19 data sets are treated as emulated defects. With 12 chips, there is a total of 12*19 = 228 defect-free data sets and 12*1800 = 21,600 emulated defect data sets.

The analysis is performed on pairs of local currents within each data set. Figure 5 displays the V_{DD} ports and lists the pairings possible as two subsets, *orthogonal neighbors subset* and a *cross neighbors* subset.The analysis is performed on the entire set (all pairings) and compared with the results obtained for the subset identified as *orthogonal neighbors* to determine the impact of this parameter on defect detection sensitivity.

5.3 Correlation Analysis for Variation

The primary purpose of sweeping the DESM across 19 different values is to enable a sensitivity analysis that is designed to answer questions such as: "at what DESM volt-

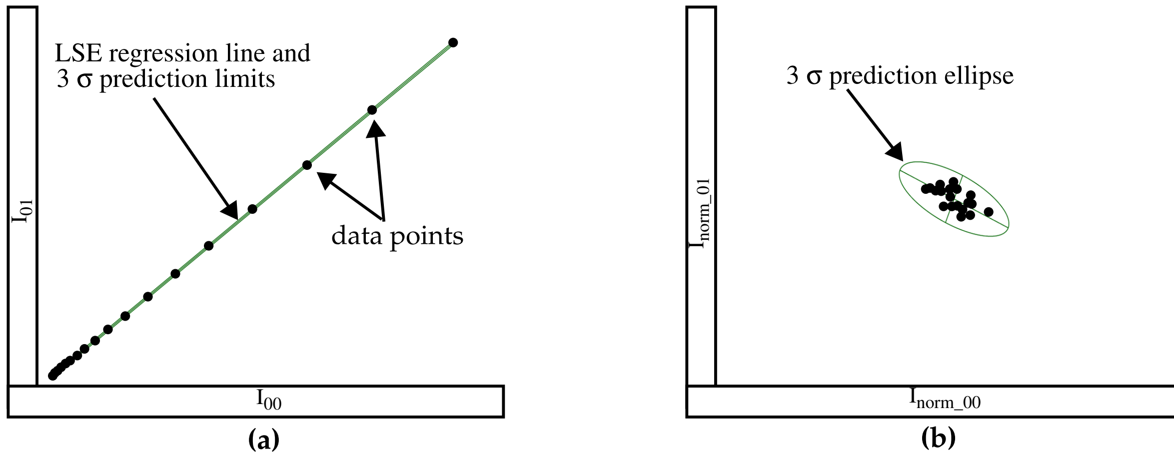

Figure 6. Chip C1 (a) I_{00} vs. I_{01} and (b) I_{norm_00} vs. I_{norm_01} scatterplot of defect-free data.

age levels can the emulated defects be detected?", and "how high is the confidence level of each positive detection?" A secondary purpose is related to problems associated with applying statistical methods to small data sets, i.e., the 12 chips. Here, we make use of the 19 defect-free data sets obtained from each chip under different DESM voltages to increase sample size. In order to remove any concerns that this may unfairly bias the results, we also give the results of an analysis that uses only one set of defect-free data from each chip.

A third purpose is related to the analysis of variance in the data. By using the defect-free data sets obtained from a single chip, it is possible to decompose several sources of variation that impact the results, e.g., variations introduced by parameters related to the test apparatus and power grid. Through a comparative analysis using the data sets from other chips, it is possible to identify the relative magnitude and significance of these sources of variations.

5.4 Correlation Analysis of Defect-free Data from a Single Chip

Perhaps the most challenging aspect of hardware experiments in comparison to simulation experiments is understanding and accounting for the various sources of signal variations. The measured parameter, I_{DDQ}, in our experiments is analog in nature and is subject to variations related to the measurement instrumentation and test apparatus, i.e., noise and series parasitic resistances, as well as those related to the chip itself, such as pin and routing parasitics and within-die and between-die process variations. It is important to understand the relative impact of these signal variation sources as well as have a means of calibrating for them.

In the context of our test methods, the most meaningful approach to decompose the sources of signal variations is through the analysis of variance in scatterplots. There are two types of scatterplots that are of interest in our analysis. The first type is constructed using *absolute* local currents while the second type is constructed using *normalized* local currents. For example, Figure 6(a) plots the absolute local currents, I_{00}, along the *x* axis against the corresponding I_{01} on the *y* axis for chip C1. The plot includes 19 pairs of values, one pair for each of the DESM voltages. In contrast, the scatterplot of Figure 6(b) shows the same data except that each of the local currents is first divided by the global values that were measured simultaneously, as described in Section 5.1. The effect of the normalization operation is to remove the magnitude of the absolute current from consideration. In other words, the dispersion of the data points along the line as portrayed in Figure 6(a) is eliminated, and the data points are effectively clustered together in a blob as shown in Figure 6(b).

Standard methods for the analysis of variance are applied to these types of scatterplots. For the data shown in Figure 6(a), *linear regression analysis* is applied by computing a best fit line through the data points and a set of 3 σ prediction limits. The analysis of variance of the data in Figure 6(b) is accomplished using a *prediction ellipse* method. The elliptical bound around the data points is computed from the eigen values of their covariance matrix and a 3 σ X^2 (chi-square) distribution statistic.

The data points in Figure 6(a) are nearly co-linear, yielding prediction limits that are very narrow. This is expected since the data is derived from a single chip, and therefore, several important parameters that introduce dispersion of the data points are held constant, such as the series resistance between the power supply and the V_{DD} ports, and on-chip parameters related to process variations. The sources of variation that remain are those related to environmental changes such as temperature and noise. Temperature variations are minimized by collecting both data points in each pair close together in time as described earlier. Therefore, most of the variation is due to noise. The

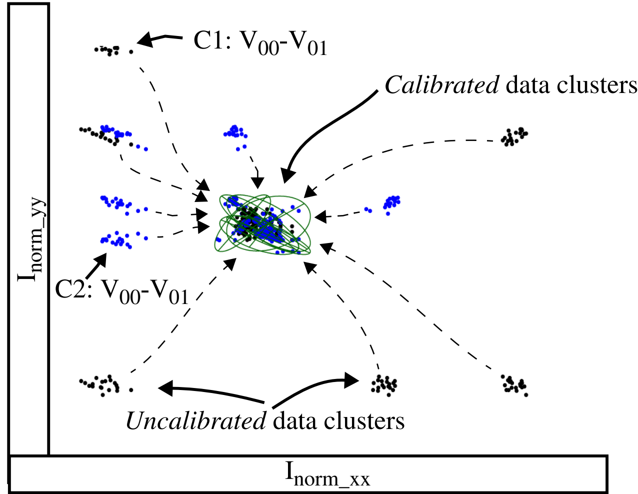

Figure 7. Chips C1 & C2, all pairings of I_{norm}, *uncalibrated* and *calibrated*

noise floor under the existing test setup is approximately 300 nA.

Similar conclusions can be drawn from the data displayed in Figure 6(b) except that the dispersion is more pronounced. This is due, in part, to the difference in scaling factors used to plot the data. However, the dispersion is actually larger than that present in the scatterplot of Figure 6(a). In this case, the normalization operation is responsible for increasing the dispersion because the divisor, i.e., the global current measurement, is also subject to noise. Moreover, the global context of the measurement, i.e. the entire array, is subject to a wider range of process variations than the regional context associated with two local measurements. As will become evident in the defect sensitivity analysis given in the following sections, these elements can reduce detection sensitivity of small defect currents.

5.5 Correlation Analysis of Defect-free Data from Two Chips

The data shown in Figures 6(a) and (b) is drawn from a single chip, and therefore is not representative of an actual testing environment, in which the data that defines the defect-free behavior of the chip would be drawn from a much larger sample of chips. When this is done, the other sources of variations that are not present in the single chip analysis will impact the level of dispersion of the data points in the scatterplots.

This is more clearly illustrated using ellipse analysis than regression analysis. Figure 7 plot normalized leakage currents from two chips, C1 and C2, for all 6 pairings of V_{DD}s. The clusters of data points around the periphery of the plot represent the data as measured. For example, two of the *uncalibrated* data clusters are labeled $C1{:}V_{00}\text{-}V_{01}$ and $C2{:}V_{00}\text{-}V_{01}$ and represent data from the same pairing in the two chips. Although the ellipse needed to enclose both clusters of data points for this pairing is not shown, it is clear that its size would increase significantly over that shown for C1 in Figure 6(b).

The displacement of the clusters from each other is caused primarily by variations in the series resistance between the power supply and each of the attachment points to the power grid. Variations in series resistance can occur in either of the wire segments that define these paths, namely, the segment between the PWR supply and the V_{DD} ports on the packaged chips, and the segment between the V_{DD} ports and the power grid within the package and chip. Since the same test apparatus is used to collect data from both of these chips, the resistance variations along the first segment are nearly zero. Therefore, the differences in series resistances must occur along the second segment, i.e., within the package and chip or as contact resistance variations in the clam-shell style ZIF socket on the test board.

As indicated, the area enclosed by the ellipse would increase significantly if this type of variation is not corrected for. In previous work, we developed and demonstrated a “probe card calibration” (PCC) technique designed to reduce this type of variation [7]. The heads of the dashed arrows show the result of applying PCC to the data clusters shown around the periphery in Figure 7. The clusters from both chips have been linearly displaced to the center of the figure. The 3 σ prediction ellipses shown in the figure are derived using the combined data sets. Minimizing their size is desirable because, as we will show, defect detection sensitivity is strongly correlated to the level of dispersion in the defect-free data clusters.

5.6 Defect Current and Background Leakage in the Test Chips

One important advantage of measuring local currents at each of the supply ports is the increased level of observability afforded by such methods. Here, observability refers to the ability to distinguish between the current drawn by a defect and normal background leakage current. For example, if a chip contains 100 power ports, then the leakage current through any one V_{DD} port will be approximately 100 times smaller, on average, than the leakage current measured globally. Therefore, the probability of detecting a defect can be much higher by measuring the local currents, particularly in large chips which incorporate large numbers of V_{DD} ports.

The chips used in this research contain 4 V_{DD} ports. Although it is not possible to reveal the actual magnitudes of the defect and leakage currents, the ratio of defect current to leakage current is reported and serves to demonstrate the claim that defect observability is enhanced.

Table 1 lists mean values of the ratios of total defect

current to global background leakage in columns two and three, respectively, for 18 DESM voltage levels given in column 1. The defect currents used in the numerator of the ratios are measured through the DESM as follows. First, all defect emulation transistors are turned off and the DESM current is recorded. This represents the leakage current through the defect emulation transistors at this particular DESM voltage. Second, the DESM current is measured as each of the defect emulation transistors in the 100 TCs is enabled, one at a time, and the leakage value is subtracted. The difference yields only that portion of the DESM current that passes through the *enabled* defect emulation transistor, which is the value we are interested in. The mean value used in the numerator is the average across the 100 TCs and the 12 chips. The denominator in each ratio is the average global leakage value (all defect emulation transistors turned off) as measured through the GSM across the 12 chips.

DESM (V)	MEAN I_{def}/I_{leak}	PROJECTED 1 cm^2 chip
0.85	0.72	0.006
0.80	1.33	0.011
0.75	1.83	0.016
0.70	2.24	0.019
0.65	2.55	0.022
0.60	2.75	0.024
0.55	2.89	0.025
0.50	2.94	0.025
0.45	2.93	0.025
0.40	2.85	0.024
0.35	2.72	0.023
0.30	2.55	0.022
0.25	2.34	0.020
0.20	2.11	0.018
0.15	1.87	0.016
0.10	1.64	0.014
0.05	1.42	0.012
0.00	1.21	0.010

Table 1: Defect current to leakage current ratios in the test chips.

The range of the mean ratios varies from 0.72 (harder to detect) to 2.94 (easier to detect). At first glance, it may appear that the larger mean ratios should be easy to detect using traditional I_{DDQ} methods, e.g., the ratio 2.94 is nearly 3-to-1 defect current to leakage current. However, in the context of a larger chip, this would not be the case. In order to illustrate this, column four of Table 1 lists the projected ratios for a chip approximately 1 cm^2 in size.

The 1 cm^2 hypothetical chip contains 468 copies of the TC array and contains a 27x19 area array of power ports. As a conservative estimate, the ratios given in column two are scaled in column four by 468/4 = 117. The factor of 4 provides an allowance for re-distribution of defect and leakage current in the larger array that adversely impacts detection sensitivity[1]. Using these assumptions, the smallest projected ratio is 0.006, as given in the first row of the table for the DESM voltage of 0.85 V. This indicates that the defect current measured in our experiments would be over 160 times smaller than the leakage current in the hypothetical chip. In specific cases in our experiments, it was possible to detect defect current in ratios smaller than the values shown in the table by a factor of 4, and we believe this factor could be as large as 10 if signal-to-noise ratios are improved.

6.0 Emulated Defect Detection Results

6.1 Data Analysis

The defect detection procedures are formulated on the analysis of scatter plots, such as those shown in Figures 8(a) and (b) for regression and ellipse analysis, respectively. The local currents from any one chip and experiment can be paired in 6 distinct combinations, given as V_{00}-V_{01}, V_{00}-V_{11}, etc. as described in Section 5.2.

The scatterplots shown in Figures 8(a) and (b) are derived from experiments that investigate defect #0, as shown at position (x, y) = (5, 21) in Figure 4. The defect-free data used to compute the prediction limits in Figure 8(a) and the prediction ellipses in Figure 8(b) is drawn from 12 chips at each of the 19 DESM voltages for a total of 228 data points. The emulated defect data is also drawn from the 12 chips at each of the 18 DESM voltages for a total of 216 data points[2]. Samples of defect-free data and emulated defect data are labeled in each of the figures.

The scatterplots for each of the 6 pairings in Figures 8(a) and (b) have been offset along the x and y axes to assist with the visual presentation of the data. The regression prediction limits in Figure 8(a) are extremely narrow and appear as a single line in the figure. A closer inspection would reveal that the two hyperbolas representing the prediction limits are finite in width. Although it is difficult to discern in the figure, all but 2 of the defect-free data points fall within the limits and most of the emulated defect data points fall outside the limits.

1. The value of 4 is chosen assuming re-distribution causes defect current to be reduced by 1/2 and leakage current to double over that measured in a chip with one copy of the array, as is done here.
2. The same defect-free data and limits are used in the analysis of all 100 emulated defects.

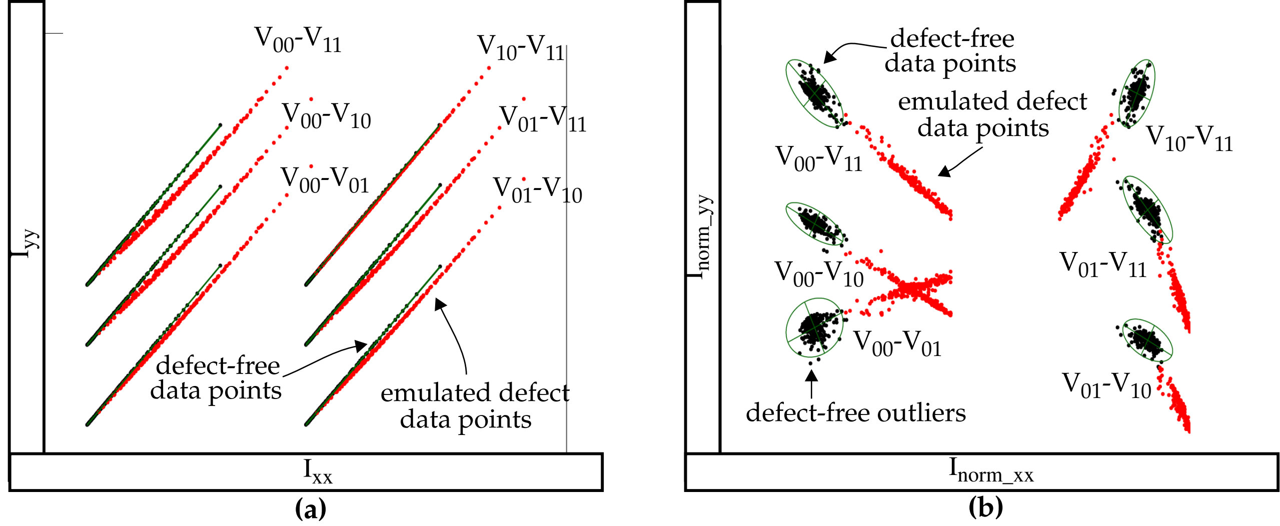

Figure 8. Regression (a) and ellipse (b) analysis of defect #0.

The ellipse prediction limits for the data clusters in Figure 8(b) are much more apparent. As shown for pairing V_{00}-V_{01}, several of the defect-free data points fall outside the 3 σ prediction ellipse, labeled *defect-free outliers* in the figure. The chips represented by these data points correspond to yield loss, as discussed below. Similar to the regression analysis, most of the emulated defect data points fall outside of the prediction ellipses.

6.2 Detection Criteria

The criteria used to decide whether an emulated defect is detected is the same for either regression or ellipse analysis and is given as follows. The defect-free data points are used to derive 3 σ prediction limits and prediction ellipses for each pairing considered in the analysis. A defect is considered detected if one or more of its data points within any pairing falls outside the prediction limits (for regression analysis) or the prediction ellipse (for ellipse analysis). It follows that an emulated defect is missed, i.e., is a test escape, if all of its data points fall within the limits across all pairings. Under this criteria, it seems straightforward to conclude that increasing the number of pairings increases the chances of detecting the emulated defect. However, increasing the number of pairings also increases the chances that defect-free data points fall outside of the 3 σ limits, and contribute to yield loss.

In order to evaluate the impact of the number of pairings, the analysis is performed over two pairing sets. As described in Section 5.2, the analysis is performed over all pairings and the subset identified as *orthogonal neighbors*.

6.3 Test Escape and Yield Loss Analysis using all Defect-free Data

Regression and ellipse analysis are performed using the defect-free and emulated defect data sets from 12 chips. As discussed in Section 5.2, we can “artificially” increase the sample size of the defect-free data sets by considering the tests performed at each of the 19 distinct DESM voltages as a separate chip. Under these conditions, the number of defect-free data sets increases from 12 to 228.

For regression analysis, the inclusion of the additional data sets improves defect sensitivity, because the wider range of leakage currents produced across the different DESM voltages increases the spread of data points along the *x* axis in the scatterplots. As long as the dispersion is small around the regression line, this characteristic tends to keep the prediction limits small along the entire length of the regression line.

In contrast, for ellipse analysis, the inclusion of the additional defect-free data sets weakens the defect sensitivity of the method, particularly when the data sets associated with lower signal-to-noise ratios are included, i.e., those associated with the larger DESM voltages. This is true because the dispersion captured by the ellipse is defined by the worst case dispersion across the entire range of values measured. The larger dispersion added by the lower defect-free currents adversely affects the detection sensitivity of defects that produce larger currents. This does not happen with regression because separate limits are defined and preserved along the *x* axis for each current level in the defect-free data.

Table 2 gives the results of regression and ellipse analysis using the pairing subsets described in the previous section. The pair of numbers reported in each cell of the table corresponds to the number of emulated defects that are *not* detected (test escapes) and number of defect-free chips that fail the test (yield loss), respectively. As indicated previously, 21,600 emulated defects and 228 defect-free chips are tested. The ideal result is 0/0, no test escapes and no yield loss.The regression analysis results are clearly superior to the results of ellipse analysis, and overall, regression

performs very well, e.g., missing less than 1% of the emulated defects and having less than 1% yield loss. Figure 9 graphically portrays the distribution of test escapes in a 3D plot in which the (*x*, *y*) plane represents the TC array, as shown in Figure 4. The height of the bars represent the number of times the emulated defect at that position is missed. It is clear that the bars are zero in all cases except for the emulated defects in the center portion of the grid. The defect number identifiers (as defined in Figure 4) given above five of the bars are the emulated defects most often missed[1]. Moreover, these are the only defects that are missed at DESM voltages smaller than 0.85 V.

test escapes (max 21,600) vs. yield loss (max 228)	orthogonal neighbors (4 pairings)	all pairings (6 pairings)
Regression	141 vs. 1	131 vs. 2
Ellipse	1143 vs. 10	1139 vs. 11

Table 2: Test Escape and Yield Loss Results

All of the emulated defects that are missed under either regression or ellipse analysis are located in the center portion of the power grid. This region of the grid distributes the emulated defect's current nearly equally among the surrounding V_{DD} ports. The lack of an anomalous local current variation cannot be distinguished from global changes in background leakage current. However, in larger chips that incorporate more V_{DD} ports, the center portion of this grid would be asymmetric to V_{DD} ports outside this region. Therefore, the defects missed here may be detectable in pairings involving V_{DD}s outside this region in larger grids.

From the data in Table 2, it is clear that larger subsets of pairings reduces the number of test escapes at the expense of increasing yield loss. For example, under regression, test escapes reduce from 141 for the orthogonal neighbors subset to 131 for the all pairings set and yield loss increases correspondingly from 1 to 2. The decrease in test escapes is expected as more pairings are included in the analysis, given the detection criteria. The increase in yield loss is caused by the larger magnitude of within-chip process variations in pairings that are more widely separated in the layout. The cross-correlation profile of

1. Since each defect is tested at 18 DESM voltages on 12 chips, the maximum z value for any defect is 216.

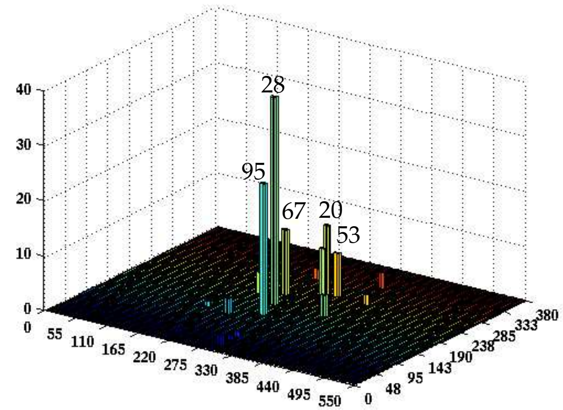

Figure 9. Location of test escapes for regression, all pairings set.

defect-free data from non-neighboring V_{DD} ports has a higher level of dispersion, which increases the chances that defect-free data points will become outliers.

6.4 Test Escape and Yield Loss Analysis using a Subset of Defect-free Data

The analysis given in Section 6.3 indicates that regression analysis is superior in terms of reducing the test escapes and yield loss. However, ellipse analysis performed under special conditions does nearly as well with 208 test escapes and no yield loss. The special condition involves restricting the number of defect-free samples used to derive the prediction ellipses to those collected with the *highest* background leakage, i.e., with the DESM voltage set to 0.0 V. Although this type of constraint is difficult to realize in production test, it serves to demonstrate the value of ellipse analysis in situations in which it is possible to obtain good signal-to-noise ratios.

As discussed in previous sections, ellipse analysis is more sensitive to noise than regression because the local and global current measurements that defines the position of the data point both posses a noise element. Under the assumption that the noise floor is independent of the magnitude of the current, it follows that the adverse impact of noise is smaller for larger magnitude currents. Therefore, prediction ellipses derived using defect-free currents of larger magnitude would be smaller.

These features are illustrated in the analysis shown in Figure 10. The defect-free data is partitioned into 19 groups of 12 data sets. Each group consists of the currents measured on the 12 chips at one particular DESM voltage. The prediction limits and ellipses are derived independently for each of the 12 point data sets and regression and ellipse analysis are performed. The results shown in Figure 10 are derived using the data from the all pairings set. The DESM voltage that was applied during the collection of the

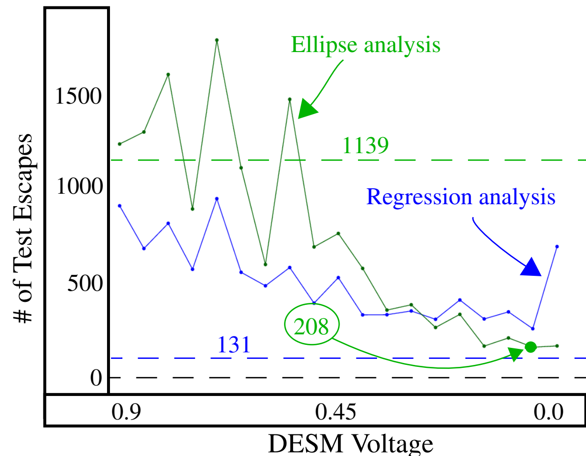

Figure 10. Number of test escapes, all pairing set with defect-free set drawn from 12 chips at each DESM voltage.

defect-free data is plotted along the *x* axis. The *y* axis gives the number of test escapes out of 21,600 emulated defects. Yield loss is zero in all cases.

In most cases, detection sensitivity increases for both regression and ellipse analysis as the background leakage current increases in the defect-free data sets. However, the best result for regression is obtained when all defect-free data is used to derive the prediction limits, as shown by the horizontal line labeled *131*, i.e., the value listed in the last column of Table *2*. In contrast, the number of test escapes for ellipse analysis are fewer than 1139 (see Table 2*)* for all cases with DESM at 0.4 V or lower. Interestingly, the number of test escapes for ellipse analysis becomes less than those shown for regression for DESM voltages less than 0.65. The best result is shown at DESM voltage 0.05 as 208.

7.0 Conclusions

The defect sensitivity of Quiescent Signal Analysis is investigated in this paper. The data from 12 test chips fabricated in a 65 nm, 10 metal layer technology are analyzed using two statistical methods, one based on regression analysis and the other based on ellipse analysis. Regression analysis applied to the data from 21,600 emulated defects is able to detect 99.4% of the emulated defects with less than 0.9% yield loss.

For the test structure under investigation in this work, regression analysis out performs ellipse analysis. Regression preserves the magnitude of the defect and leakage currents in the analysis and constructs separate bounds for different magnitudes. This feature allows regression to remain sensitive to defect currents across a wide range of defect and leakage current combinations. In contrast, the bounds for ellipse analysis are defined by the worst case variation in the defect-free leakage currents.

The results of both analysis indicate that detection sensitivity is correlated to the ratio of defect current to leakage current and is related inversely to the distance between the emulated defect and the nearest neighboring V_{DD}.

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