EXTENDED ABSTRACT

Temporal Analysis and Spatial Deconvolution of Power Pad Transients Signals for Fault Localization

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Abstract

A procedure for localizing faults to specific gates using power supply transient signals is described. The method involves deconvolving the transient signals measured at the individual C4 power ports of the chip using the impulse response functions derived for the power grid from simulation experiments. The transient signals are first partitioned into a sequence of time segments. The relevant impulse response functions are used with the time segments in a deconvolution operation to derive the individual transient signals produced by each gate along the sensitized paths under the test sequence. Anomalies in the individual gate-level transients, which are introduced by defects, are identified by comparing them with defect-free transients. The decomposition of C4 transients to gate-level transients allows the position of the defect to be isolated to one or a small group of gates. Simulation experiments are used to demonstrate the technique.

1.0 Introduction

Diagnosis is a process designed to identify the location of the fault in chips that have failed in the field or at production test. It is a key component of failure analysis. The information gleamed from failure analysis is used to tune the fabrication process for the purpose of improving reliability and yield.

Hardware-based fault localization is challenged by increases in chip complexity as well as additional interconnection levels and the limitations on the spatial resolution of imaging technology [1]. The increase in difficulty and cost of performing hardware physical failure analysis is likely to move it into a sampling/verification role. These trends continue to increase the importance of developing alternative software-based fault localization procedures.

Several “software-based” diagnostic methods have been proposed based on I_{DDQ} measurements [2-9]. These methods can be classified as static, quasi-static and dynamic diagnostic test paradigms. For static, the diagnostic test set and test response are precomputed and stored in a fault dictionary. The quasi-static paradigm, the test set is pre-computed but the fault dictionary is eliminated. Instead, the test response is computed dynamically. Under the dynamic paradigm, both the diagnostic test set and response are computed dynamically during response analysis.

In this work, we describe a novel software-based fault localization method. The basic objective of the method is to derive the shape of the transient signals generated by the individual gates or groups of gates along sensitized paths from the composite transient signals measured at the power ports or C4s of the chip. Once derived, the individual transients of the gates can be compared with those produced by a defect-free chip or simulation to identify the position of a defect.

The transients produced at the C4s are the superposition of all the individual simultaneously transitioning gates along sensitized paths under the test pattern sequence. In order to identify any anomalies in the individual gate transients, it is necessary to decompose the C4 composite transients into their constituent parts. This is accomplished by first characterizing the RC parameters of the power grid using a set of impulse response (IR) functions. The IR functions are derived from designated points in the substrate, e.g., from the power grid connections of the gates' sources, to each of the C4 ports using simulation experiments. The decomposition of the n superimposed gate transients from the measured C4 transients involves solving simultaneously the n IR functions that describe the relationship between the gate and C4 transient signals. Deconvolution is applied to eliminate the attenuation effects introduced by the RC components of the power grid. Additional gate-level resolution is achieved by partitioning the C4 transients into a sequence of time segments and applying this operation repeatedly to each set of segments.

The proposed technique provides both temporal and spatial information regarding the individual gate-level transient signals. This makes it possible to identify defects that change the shape of the gate transients, including those defects that affect only the speed of gate's output transition. Simulation results demonstrate the capability of this method for identifying defects in inverter chains of a chip with a two layer power grid.

2.0 References

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