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http://www.aue.com/aue_home.html
http://info.broker.isi.edu/1/mosis/
http://www.research.digital.com/wrl/projects/magic/magic.html
ftp://www.eecs.berkeley.edu/pub/Spice3Portion of the ISCAS85

Other simulation experiments were conducted in order to examine the SWs for defects that result in Stuck-At, Stuck-Open and Transistor Stuck-On faults such that the fault behaviors were manifested on off-sensitized paths. Thus, the logic behavior of the defective device was preserved under the test vector sequence. Experiments were also conducted with defects placed in logic gates that use redundancy to increase their current drive capability. In all cases, the effect of the defect was observable in the SWs of one or more test points.

Another set of simulation experiments was conducted where process variation was modeled globally by changing transistor gate oxide thickness and threshold voltage. In these cases, the shape of the transient SWs was preserved and only variations in magnitude were recorded. Moreover, the changes observed were consistent across all SWs. A third set of experiments were conducted in which both defects and process variation were introduced. In each case, the SWs of the defect and the process variation were superimposed and the regional variations introduced by the defects were still observable.

Conclusions: TSA offers several advantages over existing device testing techniques. The simulation experiments conducted on the c432 show that changes in the transient response of a defective circuit are observable at one or more test points and that the method is very sensitive to many types of defects. In this sense the method is based on a defect model rather than a fault model. Further, the method is not invalidated in the presence of multiple defects, requires only a small number of test vectors and can be easily adapted to on-line testing.

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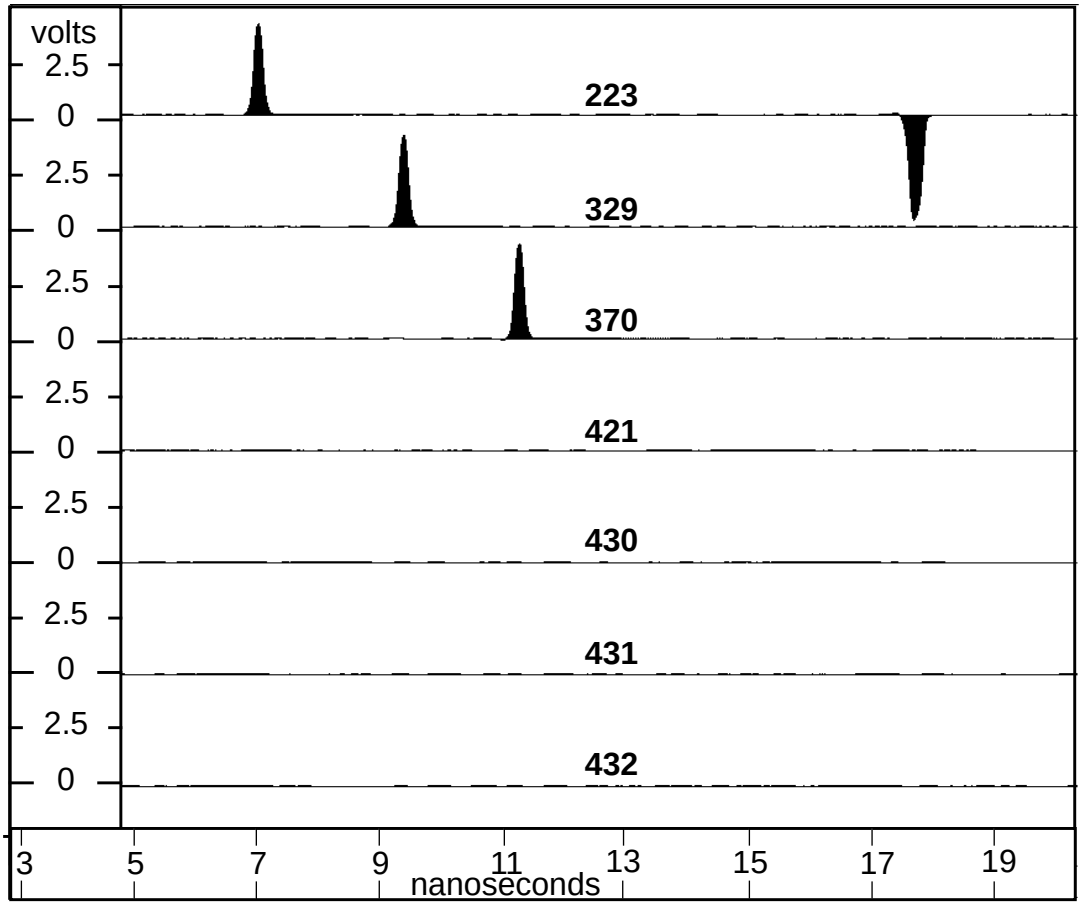

Figure 2. Voltage SWs of the c432's seven POs in the presence of the bridging defect.

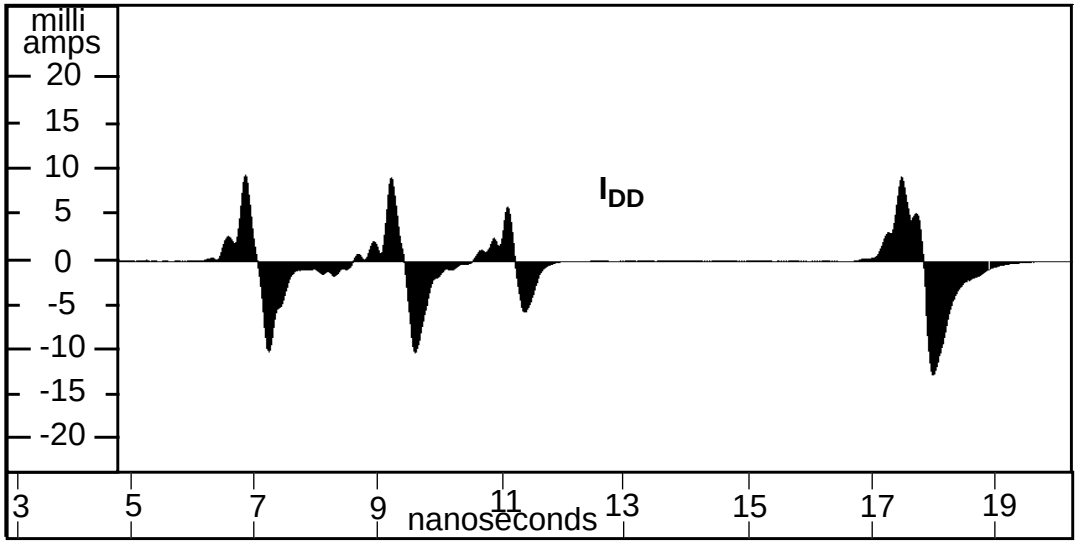

Figure 3. Current SW of the c432's supply rail in the presence of the bridging defect.

Experiments: A set of simulation experiments were conducted on defective and non-defective versions of the ISCAS85 c432 benchmark circuit. The c432 was automatically synthesized with OCTTOOLS(v5.1) using a subset of the ITD/AμE (Advanced Microelectronics Division) scmos standard-cell library(v2.2). The circuit model was created using the MAGIC(v6.43) *extract* procedure and the Hewlett-Packard CMOS26B parasitic extraction parameters obtained from MOSIS. SPICE(v3f4) simulations were run on the extracted circuits, with and without defects introduced, using the CMOS26B SPICE LEVEL=3 transistor models[7]. The test vector sequence used as input generated a high-going pulse on netlist PI line 17 through a MOSIS SCN-08 input pad. The other 35 PIs were held low. The transient voltage response of all seven POs as well as the I_{DD} transients were monitored. The raw waveforms collected were then post-processed into *signature waveforms (SWs)* by subtracting the raw waveforms produced by test devices from a set of standard raw waveforms representing a non-defective standard device.

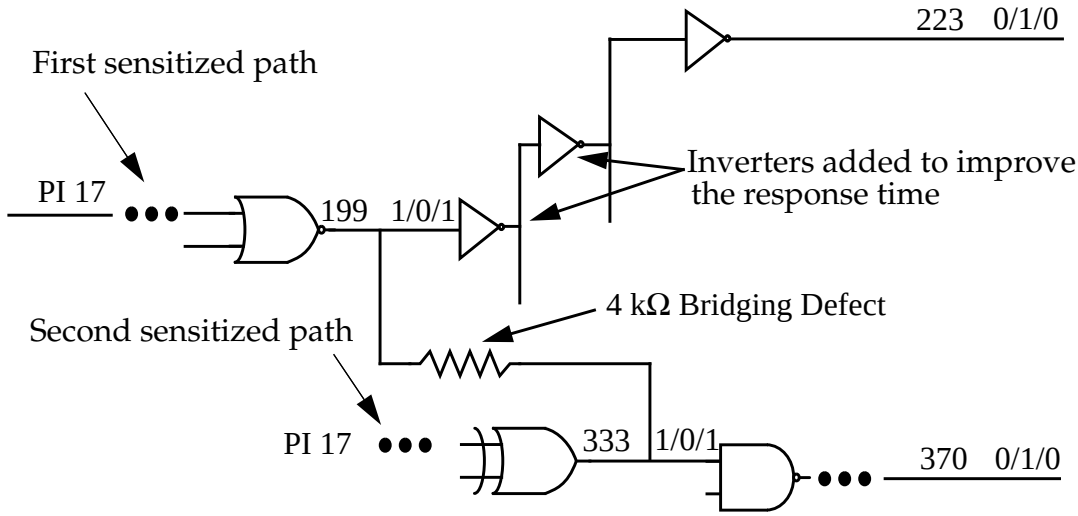

Figure 1. Portion of the ISCAS85 c432 benchmark schematic showing a bridging defect.

Results: Figure 1 shows a portion of the c432 schematic in which a 4 kΩ bridging defect has been introduced between netlist lines 199 and 333 which appeared in the layout as adjacent metal 1 lines. The changes in the logic states at the bridged nodes are identical. Therefore, neither logic testing or I_{DDQ} testing would detect this defect under the test vector sequence applied. This defect shorts the output lines of gates along two separate sensitized paths within the c432. Therefore, the logic state transitions indicated in the figure occur at different times due to the difference in the path delays from PI 17 to each of these lines. The corresponding SWs for voltage transients at all seven PO test points are shown in Figure 2 and the I_{DD} transient SW is shown in Figure 3. The ability of the technique to regionally resolve the change in the transient response is shown clearly in the SWs of POs 223, 329 and 370. The other POs were not affected. In this case, the I_{DD} SW also provides a strong indication that a defect exists.

Digital IC Device Testing by Transient Signal Analysis (TSA)

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Indexing terms: Transient response, Transient signal analysis, Digital device testing

This Letter presents a new approach to testing digital circuits that uses the variations in the transient signals generated within digital circuits as a defect detection method. The I_{DD} transients on the supply rails and voltage transients at selected test points are sampled over a test interval. Simulation experiments show that variations in the transient waveforms between defective and non-defective circuits exist and that these variations are sensitive to many types of defects even when they appear on off-sensitized paths. These variations can be analyzed using pattern recognition techniques and neural processing is proposed as the means of identifying the transient waveforms of defective devices[1][2].

Introduction: Parasitic resistance and capacitance is present in all digital ICs[3]. An ideal non-defective device can be characterized as having a well-defined set of parasitic components and therefore a predictable transient response. Alternatively, device defects add or remove parasitic elements from the AC network in the region of the defect. For example, a single open drain will remove a significant percentage of the normal parasitic capacitance present on the output node of a CMOS logic gate. Similarly, a bridging short between two or more logic gate output lines adds new parasitic resistive and capacitive elements at each of the shorted nodes. However, in real devices the stochastic nature of the fabrication process also causes variations in the values of these parasitics. Consequently, the transient response of both defective and non-defective devices varies as a function of process parameters.

In this technique, a combination of global information taken from the I_{DD} transient response and local information from several test point voltage transients is capable of identifying defective devices in the presence of process variations. Since most components are directly coupled through the supply rails, changes in the transient response can be observed by monitoring the I_{DD} transients as an input stimulus propagates from primary inputs (PIs) to primary outputs (POs)[4][5]. In many cases, the individual transistor switching transients representing the spatial variation in the parasitic networks can be temporally resolved in the resulting I_{DD} transient waveform. However, in large circuits, monitoring the I_{DD} transients alone may not provide sufficient defect resolution when a large number of transistors switch simultaneously. Defect resolution can be improved by taking advantage of the direct coupling that exists between transistors along the circuit's functional paths and the capacitive coupling that exists between adjacent conductors. Therefore, by monitoring the voltage transient at a set of test points, regional defect detection is possible. By using both the I_{DD} and voltage transients and by propagating signals from PIs to POs, defect resolution is maximized since both temporal transient behavior of the current and regional transient behavior of the voltage are used in the decision process.