Triangulating to a Defect's Physical Coordinates Using Multiple Supply Pad I_{DDQ}s: Test Chip Results

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**Chips designed while on sabbatical at IBM Austin Research Laboratory*

Abstract

Quiescent Signal Analysis (QSA) is an IDDQ method for detecting defects that is based on the analysis of multiple simultaneous measurements of supply port IDDQs. The nature of the information in the multiple IDDQs measurements also allows for the localization of the defect to physical coordinates in the chip. In previous work, we derived a hyperbola-based method from simulation experiments that is able to "triangulate" the position of the defect in the layout. In this paper, we evaluate the accuracy of this method using data collected from 12 chips fabricated in a 65 nm process.

Introduction

Diagnosis is a process designed to identify the location of the fault in chips that have failed in the field or at production test. It is a key component of failure analysis. The information gleamed from failure analysis is used to tune the fabrication process for the purpose of improving reliability and yield.

Hardware-based fault localization is challenged by increases in chip complexity as well as additional interconnection levels and the limitations on the spatial resolution of imaging technology [1]. The increase in difficulty and cost of performing hardware physical failure analysis is likely to move it into a sampling/verification role. These trends continue to increase the importance of developing alternative software-based fault localization procedures.

Several "software-based" diagnostic methods have been proposed based on I_{DDQ} measurements [2-9]. These methods can be classified as static, quasi-static and dynamic diagnostic test paradigms. For static, the diagnostic test set and test response are precomputed and stored in a fault dictionary. The quasi-static paradigm, the test set is pre-computed but the fault dictionary is eliminated. Instead, the test response is computed dynamically. Under the dynamic paradigm, both the diagnostic test set and response are computed dynamically during response analysis.

The QSA method that we propose in this work is a new approach to diagnosis and cannot be classified under these paradigms. It is complementary to these strategies and can be used in combination with them as a means of further improving diagnostic resolution. Moreover, QSA is more robust to the detrimental effects of increasing background leakage currents than these methods. This is true because, in QSA, the individual supply port currents are measured, in contrast to the global (chip-wide) I_{DDQ} measured by other methods. The partitioning of the global leakage current across the multiple supply ports of the chip reduces its magnitude in each of the supply port measurements.

In previous works, we developed statistical defect detection and localization methods using simulation experiments. In [10], a hyperbola-based diagnostic method is proposed that is able to "triangulate" a defect's location to a physical position in the layout of the chip. The method accomplishes this by computing the parameters for a pair of hyperbolas from the I_{DDQ}s measured at neighboring supply ports. The intersection of the hyperbolas identifies the predicted location of the defect in the layout.

A calibration circuit (CC) is proposed in [10] as a means of solving several problems associated with this type of localization scheme. Calibration circuits are inserted into the design at positions directly beneath the supply ports, and through scan chain control, allow for the controlled insertion of a short between the power and ground rails. The supply port I_{DDQ}s measured under the calibration tests establish upper and lower bounds on the hyperbola parameters and allow the equations to be solved. Secondly, the CC data is used to *calibrate* the supply port I_{DDQ}s measured under a failing I_{DDQ} pattern. Calibration reduces the detrimental effects on resolution caused by non-uniformities in the resistance of the power supply connections to the chip.

In this work, we elaborate and expand on the method described in [10] and evaluate its accuracy on 12 copies of a test chip. The test chips are fabricated in a 65 nm, 10 metal layer technology and incorporate an array of test structures that allow a

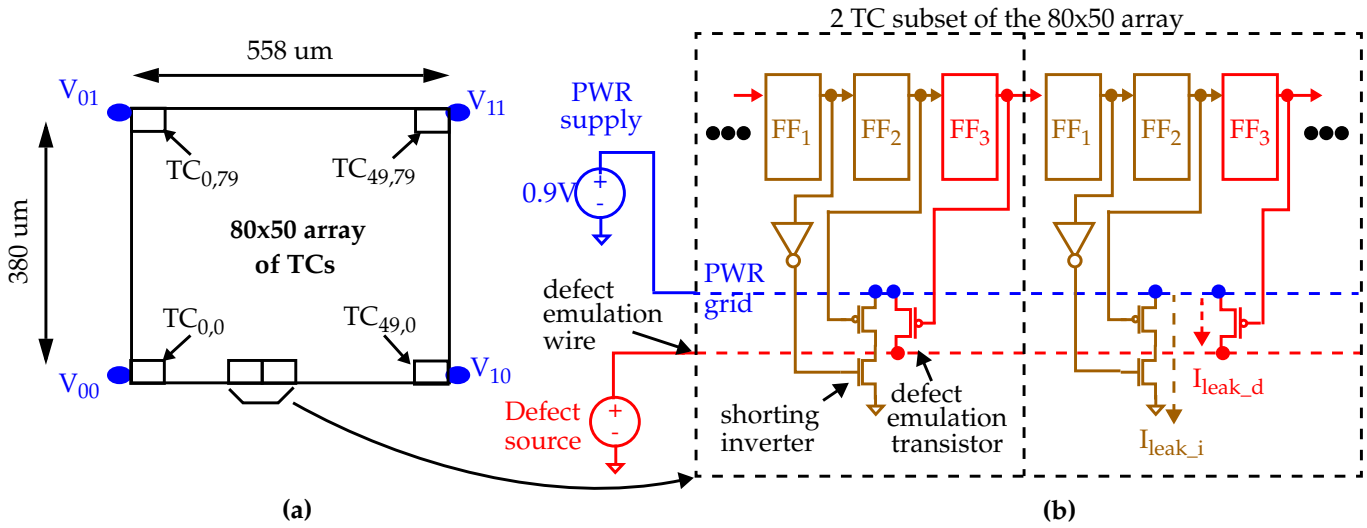

Figure 1: (a) Block diagram of the test structure and (b) and test circuit (TC) details.

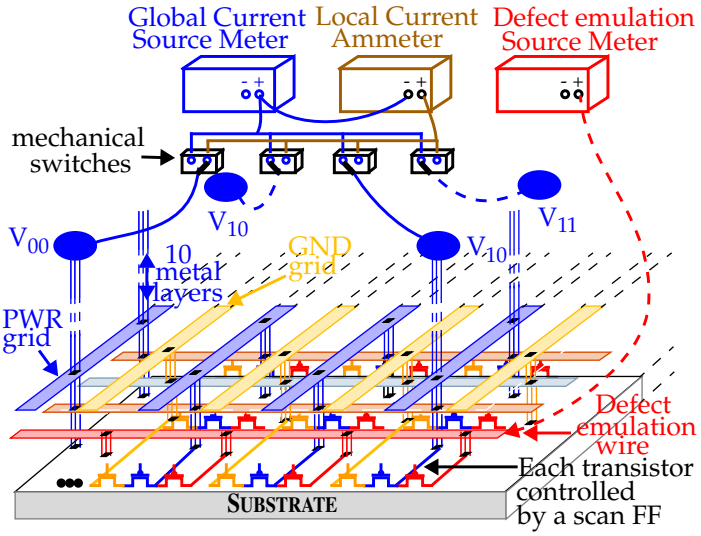

Figure 2: External Instrumentation Setup.

defect to be emulated in one of 4,000 distinct locations on the chip. The design permits control over the magnitude of the emulated defect current and leakage current. The results of our analysis show that most defects can be located to a region less than 100 microns in diameter.

Test Chip Design

A block diagram of the test chip design is shown in Fig. 1a. It consists of a 80x50 array of test circuits (TCs) that occupies an area 558 microns wide and 380 microns high. Each TC consists of three flip-flops (FFs) connected in a scan chain configuration, a *shorting inverter*, and a *defect emulation transistor* connected to a globally routed *defect emulation wire*. Fig. 1b shows a schematic diagram of two adjacent TCs. The shorting inverters and defect emulation transistors within each TC connect to the same point on the power grid.

The connection of the shorting inverters and the defect emulation transistors to power grid point sources enables introduction of two types of shorts in any one of the 4,000 TCs. The first type shorts the power grid to ground through the inverter using FF_1 and FF_2; the second type shorts the power grid to the defect emulation wire using FF_3. For the first type, the external PWR supply voltage (see Fig. 1b) defines the shorting current's magnitude.[1] For the second type, an external voltage source (*Defect source*) controls the shorting current's magnitude. Given this configuration, a defect can be emulated at any point in the array by setting the defect source to a value less than the PWR supply voltage and scanning a bit pattern into the scan chain such that exactly one FF_3 contains a 0 and the remaining 11,999 FFs contain 1s.

In addition to controlling the magnitude of the defect current, the defect source influences the background leakage current's magnitude, as measured through the PWR supply. As Fig. 1b shows, the total leakage current can be decomposed into two types, I_{leak_i} (inverter) and I_{leak_d} (defect). Given the defect emulation wire connects to the drains of 4,000 defect emulation transistors, only one of which is enabled in a particular experiment, the remaining 3,999 transistors sink leakage current from the PWR supply proportional to the magnitude of the defect source voltage. This leakage, I_{leak_d}, adds to the leakage current already present through the shorting inverters, I_{leak_i}. Therefore, we can analyze a variety of shorting and leakage current configurations by controlling the states of the defect emulation transistors and voltage on the defect emulation wire.

Figure 2 shows the external instrumentation setup. Power ports V_{00} through V_{11} wire out of the chip on separate pins in the package. The individual power pins are each wired to a low resistance mechanical switch as shown along the top portion in Fig. 2. The switch can be configured in a left or right position.

[1] In our experiments, we held the PWR supply constant at 0.9 V.

The left and right outputs of the switches connect to a common wire that routes to the *global current source meter* (GCSM) and *local current ammeter* (LCA), respectively.

The GCSM provides 0.9 Volts to the PWR grid and can measure current with a resolution less than 100 nA. The LCA is wired in series with the GCSM and allows measurement of the individual power port (*local*) currents at the same level of resolution. For example, the switch configuration in Fig. 2 allows measurement of the local V_{00} current, I_{00}, as well as the global current. The *defect emulation source meter* (DESM) sets the voltage of and measures current I_{def} through the defect emulation wire on a separate pin in the package (not shown).

Power Grid Characterization Experiments

We designed the first set of experiments to determine how power grid resistance influences local currents' magnitude. In these experiments, we disconnected the defect emulation wire, disabled the defect emulation transistors, and used the shorting inverters instead to provide stimulus to the grid.

We enabled each of the 4,000 shorting inverters from one of the chips, one at a time, and measured the global and local currents. Because we are interested in characteristics of the grid resistance and its influence on the local current distributions from layout point sources, we also performed the following steps. After testing each array element, we disabled the shorting inverter of the TC under test, measured the global and local leakage currents, and subtracted them from the values measured with the shorting inverter enabled. We then normalized these current differences by dividing them by the global current. This type of normalization virtually eliminates variations in the transistor current magnitudes introduced by process variations.

Figure 3 shows the current profile derived from the normalized local currents, I_{norm_00}. The x- and y-axes represent the (x, y) plane of the TC array and the z-axis represents I_{norm_00}. Local currents are largest near V_{00} because TCs near this location draw a larger fraction of their current from V_{00} (maximum is approximately 31percent) than TCs further removed. The range of values of approximately 11 percent shows the effect of grid resistance on current distribution to the V_{DD}s.

The smooth monotonically decreasing nature of the surface in Fig. 3 provides important "local" information that can be leveraged for detecting and localizing defects. Although we do not show the current profiles for the remaining three V_{DD}s, the same characteristic shape exists in their surfaces; only the orientation is different. A key feature present in these profiles is the one-to-one mapping between the supply port I_{DDQ}s and the position of the enabled TC in the 2-D array.

The unique mapping relationship between layout position and the corresponding I_{DDQs} enables a simple scheme for defect localization based on a *lookup table*. The lookup table maps

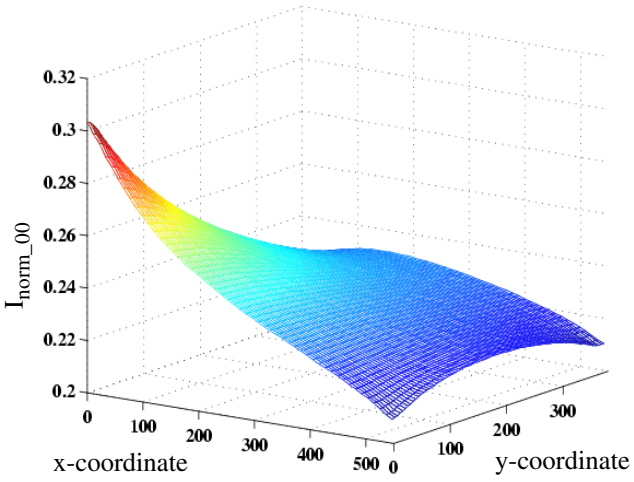

Figure 3: I_{norm_00} profile.

discrete positions in the layout to sets of supply port I_{DDQ}s. The lookup table can be derived from simulation experiments and fast power grid simulators, such as ALSIM [11]. We present results of applying this technique to a set of chips in [12]. In this work, we investigate a method based on an analytical model. We predict defect locations using only the measured I_{DDQ}s, and therefore a lookup table is not needed.

In either method, the accuracy of the localization methods are greatly improved by correcting for resistance variations in the power distribution systems of the chips. In previous work, we developed and demonstrated a calibration method capable of significantly reducing the adverse impact of these types of variations [12] and [13]. This method is applied to the I_{DDQ} data analyzed in this work.

Current Fraction Contour Analysis of the Power Grid

The smooth surface of the current profile shown in Fig. 3 suggests that normalization, i.e., division by the global current, is effective at eliminating current magnitude as a parameter in the characterization of the power grid's resistance. The elimination of the current magnitude parameter is also a desirable characteristic in a defect localization algorithm, i.e., the magnitude of the defect current should not influence the position predicted by a localization algorithm. In previous work, we demonstrated the effectiveness of a local form of normalization, in which the supply port I_{DDQ}s of neighboring V_{DD} ports are used to compute a current ratio, e.g. I_{00}/I_{01} [10]. Unfortunately, current ratios introduce non-linearity in the analytical model that complicates matters. An alternative that provides the benefit of normalization and near linearity is to compute *current fractions*, e.g., $I_{00}/(I_{00} + I_{01})$.

Figures 4 and 5 plot the current fraction contours of chip C1 for V_{DD} port pairings V_{00}-V_{01} and V_{00}-V_{10}, respectively. The x-y plane represents the TC array. The lines within each plot delimit the iso-current fraction regions, i.e., positions in the

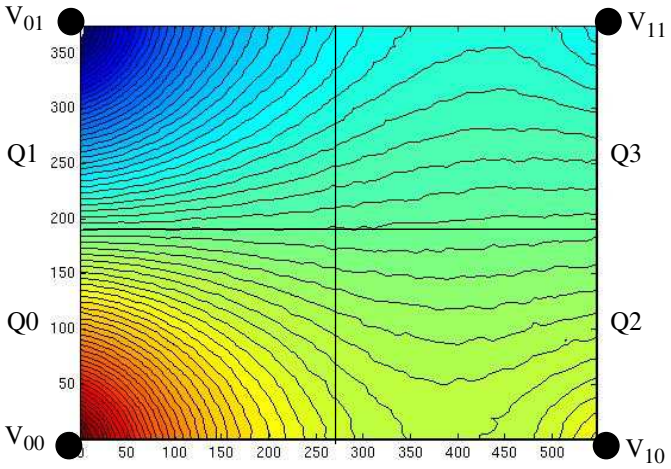

Figure 4: V_{00}-V_{01} current fraction contours.

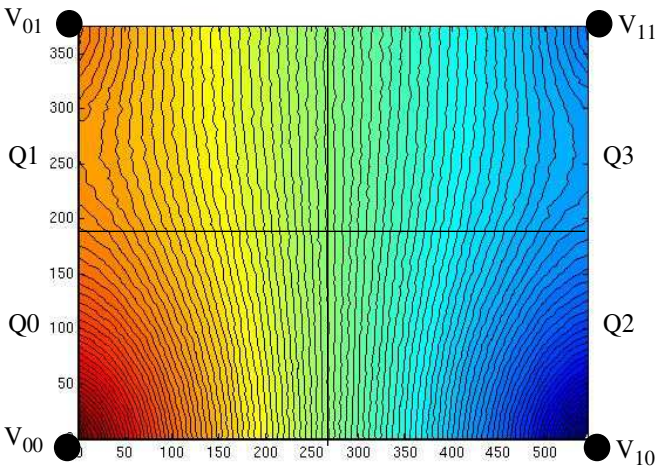

Figure 5: V_{00}-V_{10} current fraction contours.

layout that posses a similar current fraction. The current fractions are computed as $I_{00}/(I_{00} + I_{01})$ in Fig. 4 and as $I_{00}/(I_{00} + I_{10})$ in Fig. 5.

An analytical model capable of describing these curves is complicated and must take into account the influence of all V_{DD} ports in order to be complete. However, the behavior of the curves in the region surrounding the V_{00} supply port, identified as quarter Q0 in the figures, is less complex and appears quadratic in nature. Analytical models based on ellipses and hyperbolas are candidates for describing the curves in these regions. Our analysis to date has determined that hyperbolas more accurately approximate these curves but our work in this area is on-going.

Hyperbola-based Model

Equation 1 and Figure 6 define and illustrate horizontally-oriented hyperbolas, as a model for the contours curves shown in region Q0 of Fig. 5. Vertically-oriented hyperbolas, appropriate for the curves shown in Fig. 4, are similarly defined. The V_{DD} ports V_{00} and V_{10} map onto the graph at the foci, labeled F_1 and F_2 in Fig. 6. The space between the foci represents the 2-D space of the TC array.

$$\frac{(x-h)^2}{a^2} - \frac{(y-k)^2}{b^2} = 1 \qquad (1)$$

A key component to modeling the set or family of contour curves shown in region Q0 of Figures 4 and 5 is to define the relationship between them. Figure 6 defines an additional parameter c used to define the relationship among a family of hyperbolas designed to serve as models for the contour curves. A family of hyperbolas is defined as a set that share a common center and focus. The h and k parameters define the center of the hyperbolas, which corresponds to the midpoint between the foci.

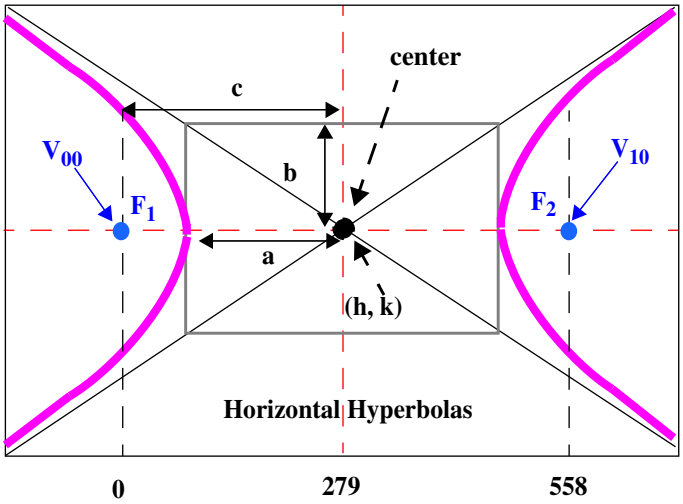

Figure 6: Definitions of the hyperbola parameters

The a and b parameters of Equation 1 shown in Fig. 6 need to be defined in terms of the current fractions. However, the c parameter allows an alternative expression, Equation 2, that eliminates b. Here, b^2 is replaced with $(c^2 - a^2)$. Parameter c is

$$\frac{(x-h)^2}{a^2} - \frac{(y-k)^2}{c^2 - a^2} = 1 \qquad (2)$$

constant for all hyperbolas in the family as the distance between their center, (h, k), and the coordinates of the power ports or foci. Therefore, only a needs to be defined in terms of current fractions.

From the diagram shown in Fig. 6, a defines the point of intersection of the $I_{00}/(I_{00} + I_{10})$ hyperbola with the horizontal line defined between the center $(h, k) = (279,0)$ and V_{00} (F_1 in the figure). Therefore, a varies from 0, at the center, to L/2 at V_{00}, where L is defined as the distance between V_{00} and V_{10} (558 for the TC array). The current ratios at points along this line

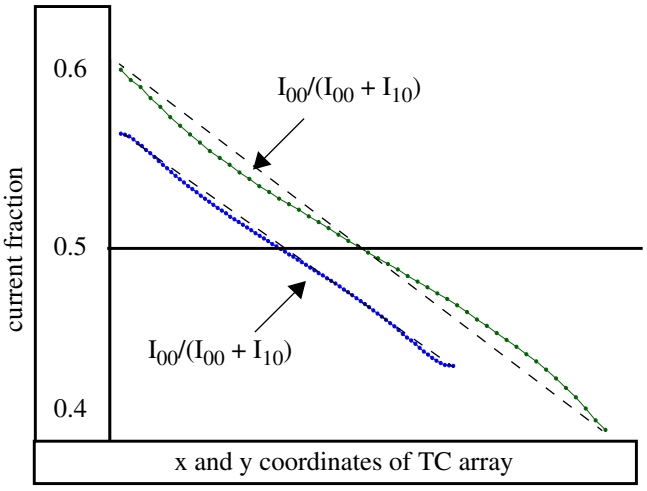

Figure 7: Current fractions along lines between V_{00}-V_{01} and V_{00}-V_{10}.

increase from 0.5 at the center to a maximum current ratio, e.g. 0.60 for $I_{00}/(I_{00} + I_{10})$ near the V_{00} supply port.

Figure 7 shows the current fractions computed from chip C1 as each of the shorting inverters are enabled, one at a time, along the lines between V_{00}-V_{01} and V_{00}-V_{10}. The x-axis represents the position of the enabled shorting inverter. The nearly linear shape of the curve reflects the uniform spacing of the contour curves along these lines in Figures 4 and 5. The linear nature of the curves allows a close approximation for a to be derived if the endpoints or bounds of the curves are known. Equation 3 can be used to derive a under these assumptions. Here, I_{ub} and I_{lb} represent the upper and lower bounds on the current fractions at the endpoints and L represents the distance between the V_{DD} ports.

$$a = \frac{L}{2} - L\left(\frac{(I_{ub} - I_{00})}{(I_{ub} - I_{lb})}\right) \qquad (3)$$

A straightforward way of obtaining the upper and lower bounds, I_{ub} and I_{lb}, is to embed calibration circuits (CCs) in the design at positions beneath the supply ports. For example, Fig. 1a identifies four TCs in the array, $TC_{0,0}$ through $TC_{49,79}$, that correspond to these positions. CCs are similar in design to the TCs shown in Fig. 1b, with only the shorting inverters present. The upper and lower bounds are obtained by enabling each of the CCs, one at a time, and measuring the supply port I_{DDQ}s. For example, the I_{ub} and I_{lb} in Equation 3 for horizontal hyperbolas are I_{00} and I_{10} measured with TC_{00} enabled.

With the bounds defined, defect localization is performed by calculating the parameter a for two pairings of orthogonally positioned V_{DD} ports, e.g., V_{00}-V_{01} and V_{00}-V_{10}. The a parameters are used in Equation 2 to derive a vertical and horizontal hyperbola. The intersection of the two hyperbolae defines the predicted position of the defect in the layout.

I_{DDQ} Defect Localization Experiments

These experiments are designed to investigate the accuracy of our defect localization methodology for defect currents and leakages that vary over a wide range of values. These objectives are better met through the use of the defect emulation transistors and corresponding defect emulation wire because both the position and magnitude of the emulated defect current can be controlled.

Data Collection Procedure

Unlike the power grid characterization experiments which tested all 4,000 elements of the TC array, these experiments tested only a 100-TC subset. Figure 8 shows the set of randomly selected TCs in the 80x50 array. The numbered positions are the TCs under investigation.

For each of the 12 chips, we performed a series of measurements for each TC under different voltage configuration of the DESM--the source meter that drives the defect emulation wire. The first experiment for each chip is the *leakage* experiment. In this experiment, we set the state of all scan chain FFs to 1, which disables both the shorting inverters and the defect emulation transistors in all TCs in the array. We then swept the DESM across a sequence of voltages, from 0.9 V to 0.0 V in 50 millivolt intervals, for a total of 19 steps. At each DESM voltage, we measured a set of four local and four global currents through the supply ports. We performed the same operation sequence with each enabled defect emulation transistor, one at a time. The four local currents and four global currents from each experiment are referred to as a data set.

Data Sets and Quarter Selection Algorithm

For each chip, the data collection procedure produces 1,919 data sets, of which 19 represent leakage data and 1900 (19 * 100 emulated defects) represent data from the emulated defect experiments. However, the emulated defect experiment with the DESM voltage set to 0.9 V is not meaningful because there is no voltage drop across the defect emulation transistor. Therefore, we treat only 18 of the 19 data sets as emulated defects. With 12 chips, there is a total of 12 X 19 = 228 leakage data sets and 12 X 1800 = 21,600 emulated defect data sets.

For each emulated defect, we compute the position of the emulated defect by selecting a pair of orthogonally positioned supply ports. The supply ports selected are those surrounding the supply port with the largest measured I_{DDQ}, called the *primary port*. The supply port with the largest I_{DDQ} identifies the *quarter* in which the defect lies. Figure 9 displays the four quarters of the TC array. For example, if I_{01} is largest in an emulated defect experiment, then V_{01} is selected as the primary port and V_{00} and V_{11} are selected as the orthogonal neighbors.

Figure 10 shows several examples of the method applied to predict the locations of emulated defects #0, #1, #4 and #28, as

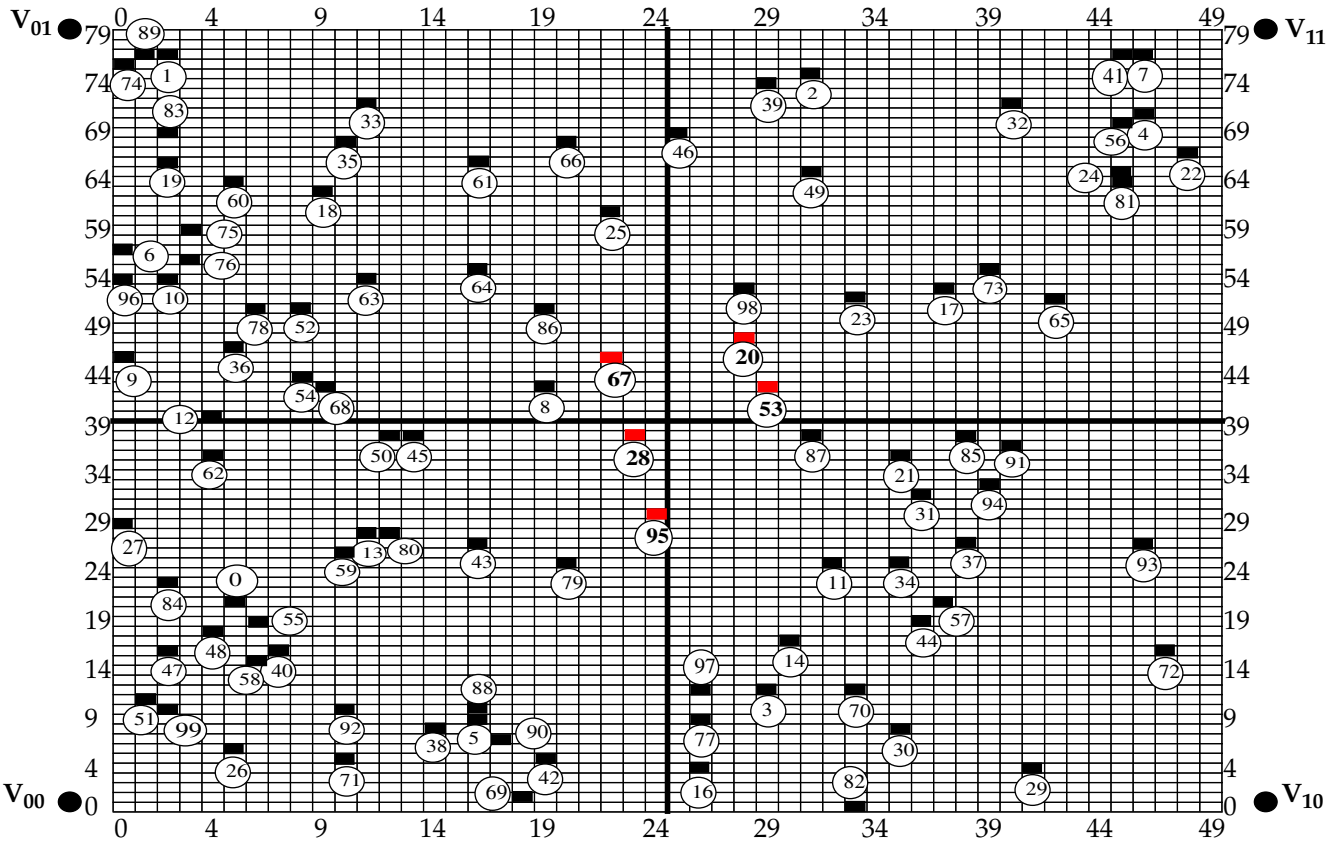

Figure 8: Positions of the 100 randomly selected TCs.

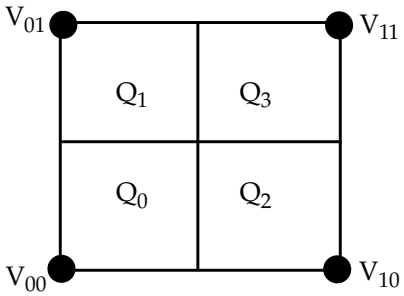

Figure 9: Quarters, Q_x, defined for the TC array.

identified in Fig. 8. For each of these emulated defects, two hyperbolas are derived, one vertical and one horizontal. The intersection of the hyperbola indicate the predicted location of the emulated defect (see defect #28 in the figure). The actual location is shown as a solid dot. The distance between the intersection of the hyperbola and the dot represents the prediction error.

Separating Defect Current and Background Leakage

The hyperbola-based localization algorithm maps the defect currents measured through each of the supply ports to an (x,y) position in the layout. Unfortunately, the currents measured also posses leakage current, which, if not subtracted, acts to "wash out" the current fractions described above and reduces the level of accuracy of the prediction algorithm.

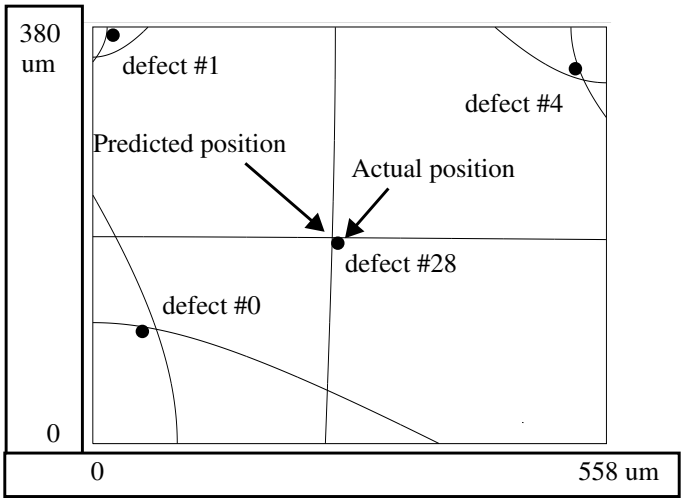

Figure 10: Example hyperbola based predictions of emulated defects.

One approach of eliminating leakage current from the measured values is through backtracking. This process is illustrated in Fig. 11. First, the leakage data from defect-free chips or simulations is used to build a profile of the leakage relationship among the V_{DD} ports. Regression analysis is applied to derive a slope of the best fit line through the pair-wise plots of leakage data. For example, the graphs shown on the right side of Fig. 11 portray a hypothetical leakage relationship for V_{DD} ports

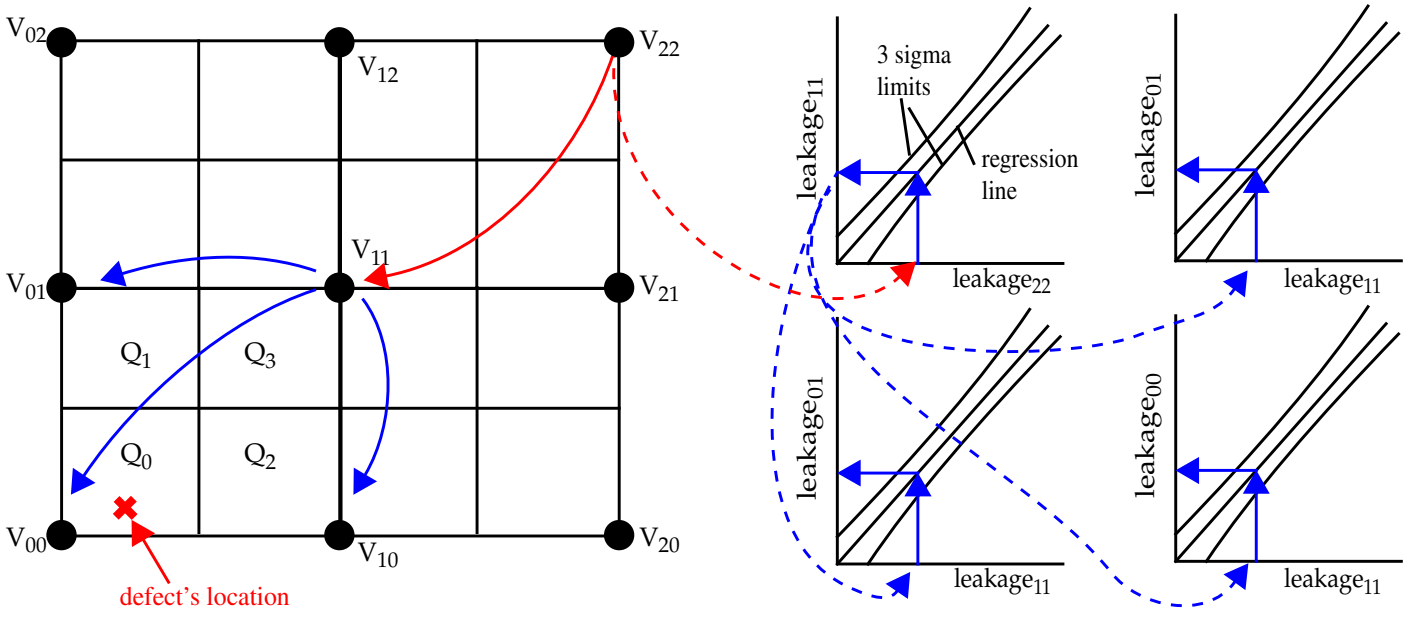

Figure 11: Backtracking method to obtain leakage.

V_{22} and V_{00} through V_{11}.

Second, the leakage components of the measured currents in a defective chip are obtained by selecting a V_{DD} port whose I_{DDQ} is minimally affected by the defect, e.g., V_{22} for the defect shown in Q0 on the left side of Fig. 11. The current measured from this port is then used in a backtracking process to obtain the leakage currents for V_{DD} ports surrounding the defect site, e.g., V_{00}, V_{01} and V_{10}. The backtracking process is shown in Fig. 11 starting with I_{22}. The dashed arrows indicate the process followed to obtain the desired leakage currents I_{00}, I_{01} and I_{10}. Last, the defect currents are obtained by subtracting the derived leakage components from the measured values.

In this work, we could not apply this method directly because of the small size of the power grid, i.e., all four supply port I_{DDQ}s possessed both leakage and defect current. Instead, Equation 4 was applied to approximate the leakage component

$$\frac{\left(I_{\text{m\_large}} - \text{leak} \times \frac{1}{S_{\text{large}}}\right)}{(I_{\text{m\_small}} - \text{leak}) + \left(I_{\text{m\_large}} - \text{leak} \times \frac{1}{S_{\text{large}}}\right)} = \text{CF}_d$$

$$\text{CF}_d = 0.5 + \frac{\text{CF}_{\text{m}} - 0.5}{\text{CF}_{\text{cm}} - 0.5} \times (\text{CF}_{\text{c}} - 0.5) \qquad (4)$$

in the measured I_{DDQ}s. The left side of the equation is a defect current fraction with I_{m_large} and I_{m_small} representing the largest and smallest I_{DDQ}s measured from two of the four supply ports. The variable *leak* is solved for and represents the leakage component of the smallest measured I_{DDQ}. The variable S_{large} is the slope of the regression line which characterizes the leakage relationship between these supply ports.

The right side of Equation 4, CF_d, approximates the defect current fraction using variables CF_m: the measured current fraction using the smallest and largest I_{DDQ}s, CF_{cm}: the current fraction computed with both the emulated defect and calibration circuit (CC) enabled, and CF_c: the current fraction computed with just the CC enabled. (Note, the CCs in these experiments are the TCs at the positions indicated in Fig. 1.) The range of the right side is 0.5 to a value close to the CC current fraction. For example, if the emulated defect is positioned mid-way between the supply ports, the largest and smallest I_{DDQ}s are similar and (CF_m - 0.5) is 0 yielding CF = 0.5. If the defect is positioned close to a CC, then (CF_m-0.5) ~= (CF_{cm}-0.5) and the right side becomes CF_c.

Application of this formula approximates the leakage current component in the smallest measured I_{DDQ}. Backtracking is used to obtain the leakage components in the other measured supply port I_{DDQ}s. The leakages are subtracted from the measured values to obtain the defect current components used in the localization method.

Localization Results

We applied the hyperbola-based localization method to the 21,600 emulated defect data sets to determine its accuracy. Accuracy is evaluated by computing the error, given as the Euclidean distance between the actual position of the enabled TC (emulated defect) and the position given by the intersection of the hyperbolas. This error is converted into a percentage by dividing it by 675 um, the Euclidean distance across the diago-

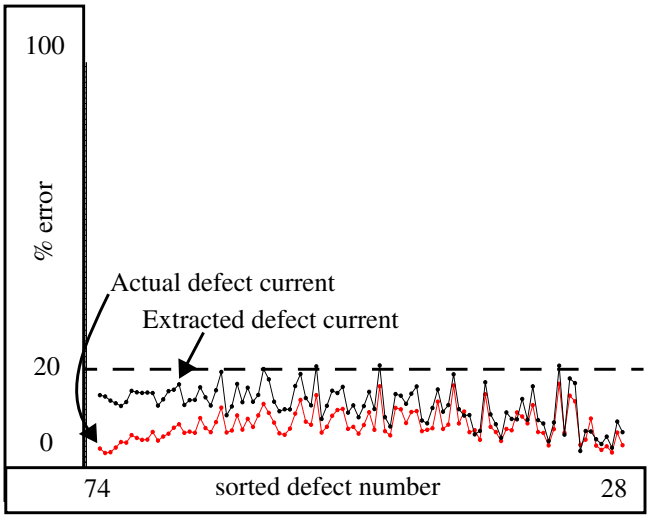

Figure 12: Chip C2: Linear equation prediction results.

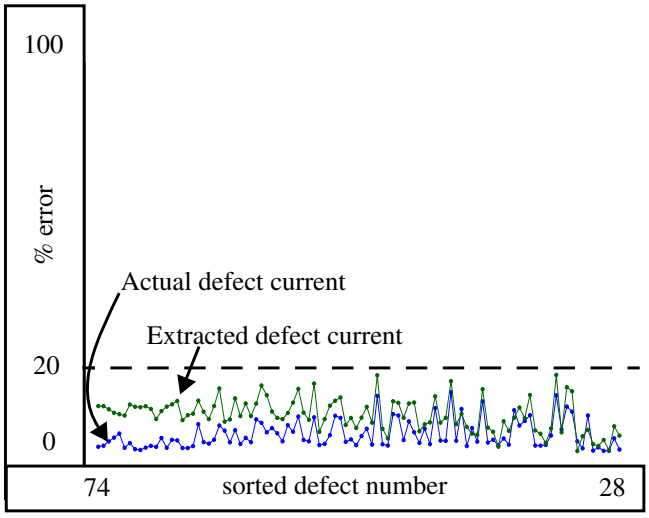

Figure 13: Chip C2: Curve derived prediction results.

nal of the array. Therefore, a 1% error is equivalent to an actual error of 6.75 um.

We explored two independent parameters of the method. In Section "Separating Defect Current and Background Leakage", we described a method and a formula to *extract* the defect current component from the measured I_{DDQ}s. The control structure within the array allows the emulated defect to be disabled and the leakage to be measured. Therefore, it is possible to compute a precise value of defect current. We perform the analysis using the extracted and actual defect currents to determine the fraction of the error added by the extraction method.

In Section "Hyperbola-based Model", we gave a linear expression to compute the *a* parameters for the hyperbolas. However, the actual behavior of *a* has a non-linear component, as shown in Fig. *7*. We perform the analysis using the linear expression and the actual *a* curves in order to evaluate the fraction of the total error introduced by the linear approximation. In total, four analyses are performed. The largest errors occur in the analysis that uses the linear expression for *a* and the extracted defect currents, as expected. The best result is obtained using the *a* curves and the actual defect currents.

The results of applying the defect localization method to chip C2 are shown in Figures 12 and 13. The emulated defect numbers shown in Fig. 8 are sorted and plotted along the x-axis and the percent error is plotted along the y-axis. The criteria for sorting is distance to the primary supply port, e.g., the results shown on the left side of Figures 12 and 13 are closer to a V_{DD} port while those listed on the right side are closer to the center of the grid. The numbers of the two emulated defects that represent the extremes are given in the figures as 74 and 28 (see Fig. 8).

As indicated in Section "Data Sets and Quarter Selection Algorithm", 1,800 emulated defect experiments were performed on each chip. For each emulated defect site, we varied the magnitude of the defect current by sweeping the DESM across 18 distinct voltages. The curves shown in Figures 12 and 13 plot only one error result for each emulated defect. The value shown is average error computed across all DESM voltages.

Chip C2 is shown because it portrays the worst case, i.e., the largest errors, among the twelve chips investigated in this work. Figure 12 gives the errors when the hyperbolas are derived using the linear expression for parameter *a*. The curve labeled *Actual defect current* gives the best result under the linear model. The curve labeled *Extracted defect current* gives the error when the defect current is estimated using the expression described in Section "Separating Defect Current and Background Leakage". Figure 13 gives the errors in an analogous way under the condition that the *a* parameters for the hyperbolas are derived using the curve data.

The figures include a horizontal dashed line that identifies 20% error. The errors for all but four of the emulated defects are below this line. In general, the errors using the curve data are smaller than those obtained under the linear model. This is expected since the curve data gives a more precise value for the hyperbola *a* parameter than the linear model. It is interesting to note that the prediction error using the *Extracted defect current* is smaller than the error obtained using the *Actual defect current* in several cases. This indicates that the hyperbola model used here is capable of only providing an estimate of the emulated defect's location. The error curve labeled *Actual defect current* in Figure 13 also supports this statement. In this analysis, the error contributions introduced by estimating both the *a* parameters and defect currents are eliminated. The error that remains is largely due to hyperbola modeling inaccuracies of the contour curves, as shown in Figures 4 and 5.

The plots in Figures 14 and 15 give the errors for twelve chips, one plot for each of the four types of analyses. The error curves

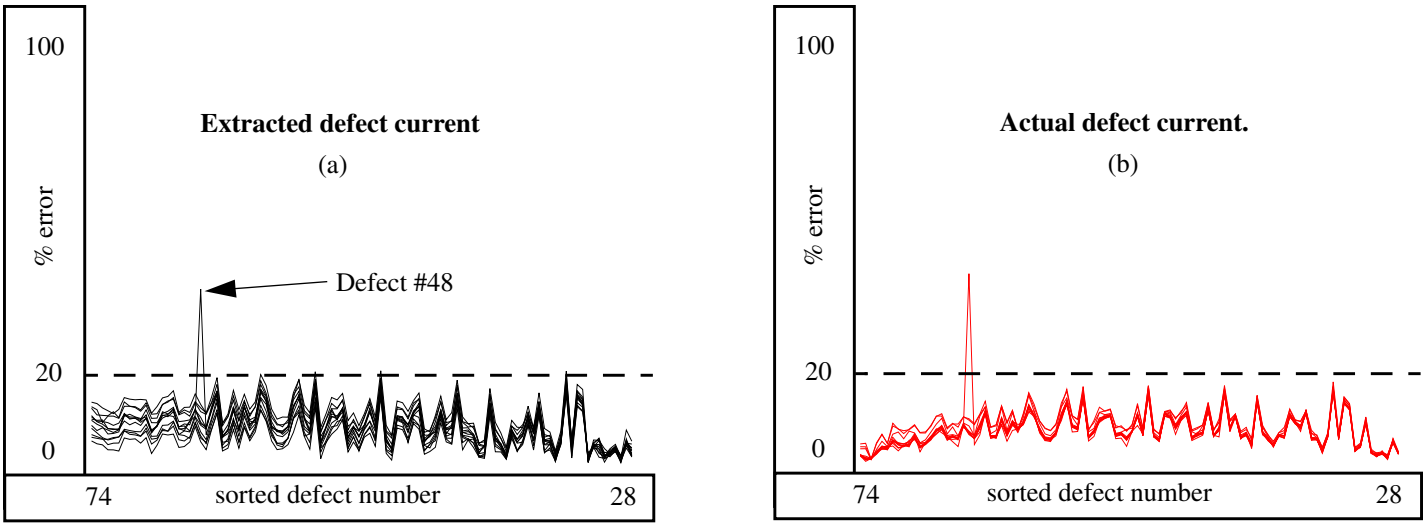

Figure 14: Prediction errors in twelve chips using linear equation.

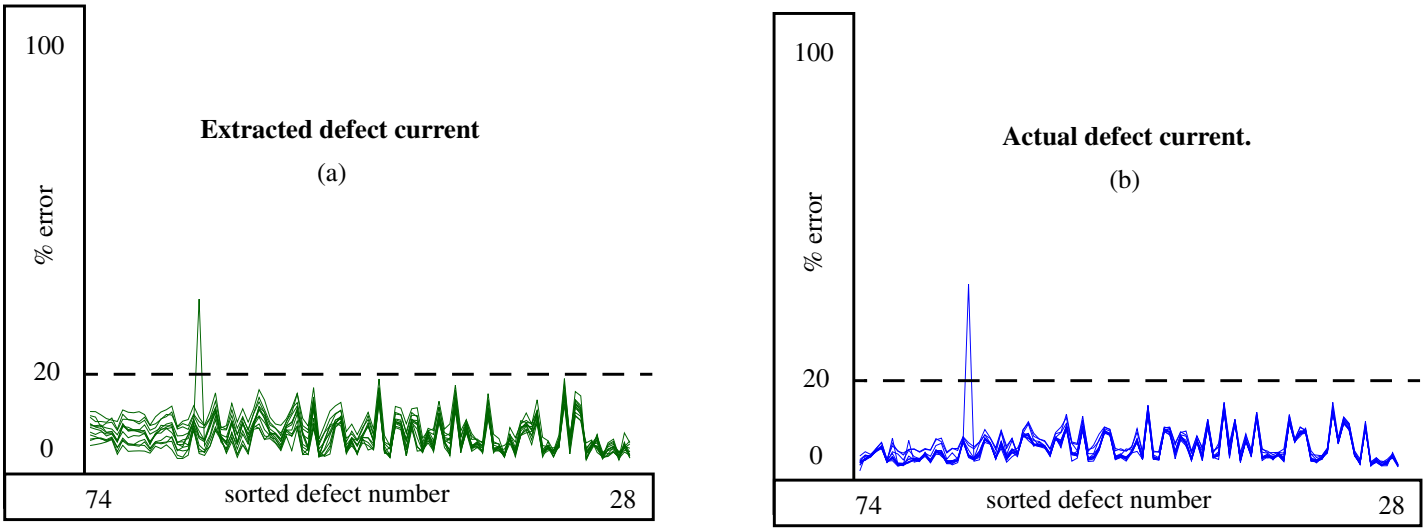

Figure 15: Prediction errors in twelve chips using a curves.

for each of the twelve chips are superimposed.

The first notable feature in the four plots is the large error for defect #48 (chip C5) of approximately 40 percent. Inspection of the data revealed that I_{01} is the largest current causing V_{01} to be chosen as the primary supply port. Under these conditions, the hyperbolas are derived in Q1 instead of Q0 (see Fig. 8). The erroneous current distribution in this sole experiment is likely the result of a corrupt scan operation. The analysis of this defect in the remaining eleven chips generated the expected result, i.e., the largest current is I_{00} and V_{00} is chosen as the primary supply port.

The plot in Fig. 14a gives the worst case error, as expected because the analysis is performed with extracted defect currents and linear equations for *a*. The variance in the errors across the twelve chips for a given emulated defect is largest in this analysis, particularly for emulated defects close to the supply ports (left portion of the plot). The smaller level of variance in Fig. 14b suggests that the expression used to extract defect current introduces this error, and is less effective at estimating the defect current component for emulated defects close to the supply ports.

Similar comments can be made with regard to the error variance in Figures 14a and 15a, i.e., the use of the *a* curves reduces the level of error variance in Fig. 15a. Here, it is also clear that the defect current extraction formula is the main contributor to the error. As mentioned in Section “Separating Defect Current and Background Leakage”, the backtracking method is preferred in chips with larger numbers of supply ports.

The errors are lowest in Fig. 15b, e.g., less than 15 percent, and the curves exhibit a high degree of consistency across the twelve chips. This latter feature demonstrates the effectiveness of the calibration technique to reshape the data to make chips of identical design appear very similar in hardware.

Summary and Conclusion

A hyperbola-based defect localization method is applied to the data collected from a set of chips fabricated in a 65 nm technology. The test chips incorporate an array of test structures that permit the controlled insertion of a shorting defect. The method uses multiple supply port I_{DDQ}s to triangulate the physical location of the defect in the layout. The results of the analysis indicate that good diagnostic resolution is achievable, with localization errors less than 15% or 100 um in most cases.

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