Detecting Delay Faults using Power Supply Transient Signal Analysis

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Abstract

A delay-fault testing strategy based on the analysis of power supply transient signals is presented. The method is an extension to a Go/No-Go device testing method called Transient Signal Analysis (TSA) [1]. TSA detects defects through the analysis of a set of power supply transient waveforms in the time or frequency domain, e.g., Fourier phase components. A recent extension to TSA demonstrated a correlation between the V_{DDT} Fourier phase components and path delays in defect-free devices [2]. The method proposed here is able to detect increases in delay due to resistive shorting and open defects using a similar technique. In particular, simulation results show that a delay defective device can be distinguished from a defect-free device through an anomaly in the Fourier phase correlation profile of the device.

1.0 Introduction

In today's competitive IC market, success often means delivering the shortest possible clock cycle. Under pressure to push increasingly complex processing technologies to the limits, designers are delivering circuits with decreased timing and noise margins. In doing so, they are making the circuits significantly more susceptible to manufacturing imperfections. In particular, previously benign manufacturing defects can now cause circuits to fail timing specifications. The "accidental" coverage of these unmodeled delay-related defects provided by functional test patterns is likely to be significantly reduced under a less aggressive structural test methodology.

A defect-oriented test method is based on a fault model that accurately abstracts some fraction (ideally all) of the analog circuit deviations introduced by defects to a set of discrete faults, that can be targeted by a set of tests and detected by production test and measurement equipment [3]. Such a method is particularly valuable if it can be demonstrated that it is capable of detecting defects that no other method in the test suite can detect. Resistive shorting and open defects are two types of defects that traditionally have not been targeted. For example, they are not easily detected using structural Stuck fault tests, particularly in cases where the value of the defect's resistance does not cause a catastrophic failure, but rather only increases delay along one or more paths in the circuit. I_{DDQ} targets shorts but is becoming increasing difficult to use effectively due to the masking effects of subthreshold leakage currents. Delay fault test methods target defects in these classes but reliable delay fault tests are difficult to derive and the size of the test pattern set is usually large.

In this paper, the capabilities of a method defined in previous work called Transient Signal Analysis or TSA, is investigated as a means of detecting increases in delay resulting from resistive shorting and open defects. In TSA, a set of power supply voltage transients (V_{DDT}s) are analyzed in both the time and frequency domain. The use of the power supply pads improves internal node observability without impacting existing design flows. The multiple test signals (measured simultaneously at several supply pads) provides the basis on which a process and technology-tolerant pass/fail metric is defined.

In previous works, a regression-based pass/fail classification scheme for TSA was derived from experimental hardware and simulation data [1]. This technique was extended in [2] for the purpose of predicting critical path delay. However, the analytical framework that describes the basis of the regression model, e.g., the relationship between path delay and Fourier phase, has not been addressed in previous works. Since the model is key to the delay-fault detection strategy described in this paper, a section is devoted to identifying the key steps of its derivation.

The main contribution of this work is to determine the sensitivity of TSA to defects that increase path delays. Delay-oriented defects were investigated in previous works but the value of the resistance associated with these defects was not explored as a parameter of the experimental space. In this work, defect resistance, type and location are varied simultaneously with process parameters in simulation experiments. Here, it is shown that one of the major effects of a delay defect is to introduce uncorrelated phase shifts in the supply pads V_{DDT} signals that are topologically close to

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the path(s) affected by the defect.

The rest of this paper is organized as follows. Section 2.0 outlines some related work. Section 3.0 describes the analytical basis of the regression model and the technique used in TSA. Section 4.0 describes the device and simulation experiments. Section 5.0 presents the experimental results and Section 6.0 gives a summary and conclusions and discusses areas for future investigation.

2.0 Background

Techniques based on the analysis of transient signals are described in [4-9]. The main drawback of these techniques is that they do not account for vector-to-vector or process variations. Therefore, they are not directly applicable to devices fabricated in deep sub-micron technologies, in which these types of variations are significant and must be accounted for.

A recent I_{DDT} work is based in principle on the process calibration technique that we have proposed for TSA [10][11]. However, calibration is performed in this technique across test sequences rather than within a single test sequence, and therefore the method does not calibrate for vector-to-vector variations. Another drawback of this techniques is that it is based on the time domain analysis of a single power supply measurement, and therefore, does not scale with chip size.

The results of research in [12] suggest that defect detection metrics based on RMS values of I_{DDT} are best accompanied by frequency metrics. Although the experiments were performed on analogue devices, enhanced detection of resistive bridges and opens was possible when the I_{DDT} RMS value was used in combination with the first five Fourier Magnitude components. A method that additionally considers the effects of process parameter variations is proposed in [13].

The technique proposed in this work differs from previous work in several significant ways. First, the method explicitly accounts for process and vector-to-vector variation effects by cross-correlating the power supply transient signals measured at multiple supply pads simultaneously. This attribute addresses the scalability of the technique to larger devices. Second, instead of Fourier magnitude and/or RMS values of I_{DDT}, TSA focuses on the analysis of Fourier phase harmonics. This choice is motivated by previous work which suggests that this representation is best at tracking process variation effects. Lastly, the method proposed here "tracks" process variation effects but does not eliminate them. This attribute allows device parametric attributes, such as delay, to be correlated across test sequences, further reducing of possibility of test escapes.

3.0 Experimental Method

Any technique based on the analysis of analog signal measurements must "calibrate" for process and technology-related variation effects, since the inability to do so can result in yield loss. TSA accounts for these effects explicitly through the cross-correlation of multiple supply pad transient signals measured simultaneously as a test sequence is applied to the primary inputs.

The supply rail's resistance and capacitance (RC) characteristics make it possible to use the static or dynamic signals as a means of distinguishing between defective and defect-free devices. The global nature of process and technology-related variation, such as changes in polysilicon resistance and transistor threshold voltages, produce *correlated* V_{DDT} signal variations in all supply pad measurements. In contrast, the V_{DDT} variations produced by a defect affect the supply pad measurements closer to the defect site more dramatically than supply pad measurements further removed. The RC attenuation characteristics of the supply grid make it possible to measure these *uncorrelated* signal variations. TSA uses correlation and regression analysis as a means of tracking process variation effects and detecting the regional signal variations caused by defects.

In previous works, a strong correlation in defect-free devices was found in the Fourier phase components across a set of power supply V_{DDT} measurements [1]. A recent work demonstrates that these components are additionally correlated to the path delays in defect-free devices [2]. Therefore, they are a natural candidate for detecting delay-oriented defects. The following sections describe the Fourier properties relating delay and phase and the TSA procedure designed to track defect-free device phase correlations as well as the anomalies introduced into them by defects.

3.1 An Analysis of Delay and Fourier Phase

The analysis of path delay and the Fourier phase components of an I_{DDT} waveform is decomposed into two parts. The first part shows the intuitive relationship between path delay and features in the individual I_{DS} waveforms generated by the gates along the path. The second makes use of a Fourier property to show the relationship between variations in the composite, I_{DDT}, waveform (due to process) and phase shifts in I_{DDT}'s frequency domain components. Due to space limitations, the analysis is performed graphically using simulation data. Refer to [14] for proofs, a V_{DDT} analysis and other details.

The relationship between path delay and the transient I_{DS} waveforms is shown in Figure 1. The input waveforms that drive two inverters, 1 and 3, along a path of inverters is shown along the top of Figure 1. The I_{DS} transients generated by these two gates are shown in the bottom portion of the figure. Dashed vertical lines are drawn through the 50%

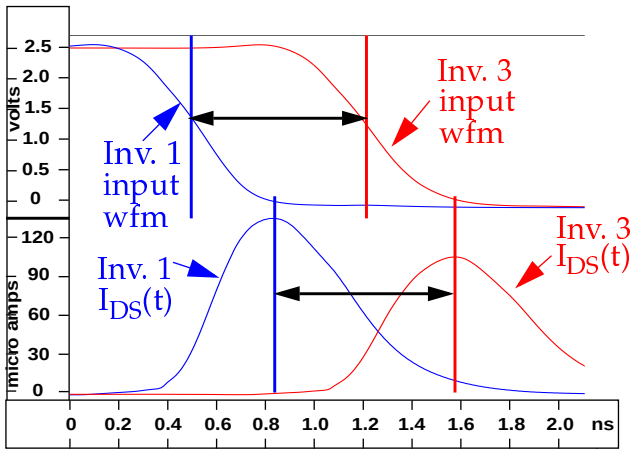

Figure 1. Input waveforms driving the 1st and 3rd inverter in a three inverter chain (top) and corresponding $I_{DS}(t)$.

points in the input waveforms and through the peak tops in the I_{DS} waveforms. The two horizontal arrows are the same length, demonstrating that path delay and the delay as measured between the I_{DS} waveform peaks are very similar. Although the latter is not an exact measure of the former, it is intuitively clear that these two quantities are well correlated due to the cause-effect relationship of the input and I_{DS} waveforms.

The I_{DDT} generated on the supply grid is the superposition (via a linear RC network) of these individual I_{DS} transients. Variations in delay, e.g. due to process variations, will cause a corresponding variation in the I_{DDT} waveform, scaling it in time by an amount closely approximated by the change in delay. However, the superposition of I_{DS} transients from multiple paths, in combination with process variations in the component values of the power grid's RC network, make it difficult to track delay using the time domain I_{DDT} signals. In these cases, the accuracy of the tracking analysis can be improved using a band of I_{DDT} Fourier phase components. This is possible because phase is related to the I_{DDT} transients through a Fourier property:

$$x(\alpha t) \overset{\mathcal{F}}{\Leftrightarrow} \frac{1}{|\alpha|} X\left(\frac{\omega}{\alpha}\right) \qquad \text{where } \mathcal{F} \text{ indicates the Fourier transform.}$$

The property indicates that scaling a time domain waveform in time scales the phase components by $1/\alpha$, proportional to frequency. Since the higher frequency components of the I_{DDT} waveform are "distorted" by interactions between multiple I_{DS} transients and the supply grid's RC component variations, the phase analysis can be focused on those frequencies that are more strongly correlated to delay, as the following example illustrates.

Figure 2 shows the I_{DDT} waveforms from simulations of a circuit (not shown) in which two paths are sensitized under three process models. (The circuit design is not important in this discussion but the interested reader can consult [14] for details). The circuit component values of the process models were obtained from MOSIS [15] for TSMC's 0.25um process. The circuit component parameters of the simulation models include BSIM transistor models and the interconnect parasitics given by MOSIS as lot averaged values. The simulation runs are labeled P#1 (slowest process) through P#3 (fastest process).

The differences in path delays along one of the paths in the circuit under process models P#2 and P#3, with respect to P#1, are -186ps and -334ps, respectively. These are the delays that we would like to track using the I_{DDT} transients. However, as indicated in the figure, the prediction of delay, given by measuring the distance at the falling edge of the I_{DDT} transients as shown in the figure, yields -169ps and -424ps, respectively. In contrast, Figure 3 shows the phase spectrums of these signals through 1.5GHz. The frequency components below ~900MHz are linear. The predictions using the phase shifts in the frequencies in the 300-900MHz band are -201ps and -324ps, respectively (see ref [14] for details on the procedure). This example illustrates that phase tracks delay, and suggests that phase can be a better estimator of actual path delay than a time domain analysis of the I_{DDT} signals.

3.2 Signature Waveforms

TSA is based on the analysis of dynamic (V_{DDT}) signals. In a production test environment, significant signal variations are generated by the test equipment through the probe tips and test head electronics. This EMI couples into the DUT's supply and distorts the transients generated by the underlying core logic. It is important to attenuate (ideally remove) these variations before passing the waveforms off to the detection algorithm. Moreover, the procedures used in TSA are based on an analysis of signal variations in the test device relative to those generated by a "golden" reference device. In order to accommodate both of these requirements, the V_{DDT} waveforms measured from the supply pads of the test device are first processed into Signature Waveforms.

Signature Waveforms (SWs) capture only the intrinsic signal variations between the devices. They are created by subtracting the waveform measured from some test point on the test device from the waveform measured from the same test point location on the reference device. This procedure can be applied to both time and frequency domain signals as shown in Figure 4. The V_{DDT} waveform from the reference (Ref) is shown along the top left plot while the V_{DDT} waveform from a test device (Test) is shown below it. Subtracting the test waveform from the reference creates

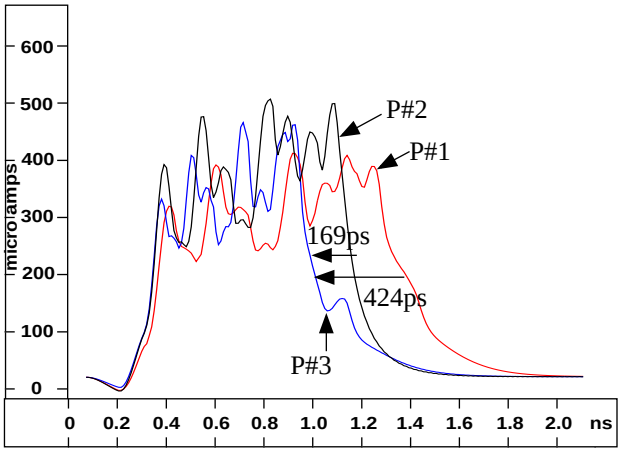

Figure 2. I_{DDT} waveforms from Process (P) simulations using circuit component values from MOSIS runs n94s(P#1), t15h(P#2) and t13o(P#3) of a circuit designed in TSMC's 0.25um process.

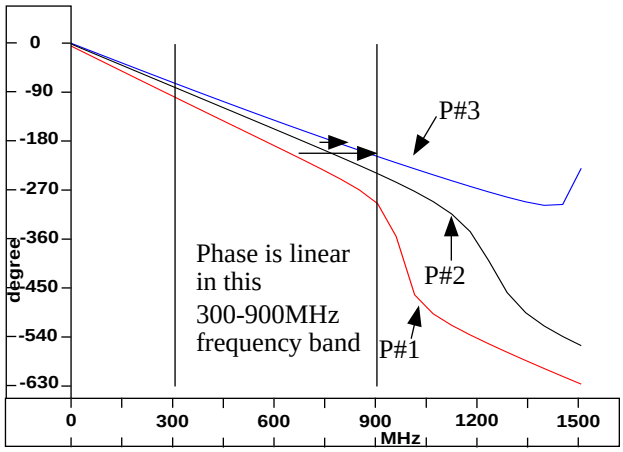

Figure 3. Unwrapped Phase spectrums of I_{DDT} waveforms shown in Figure 2.

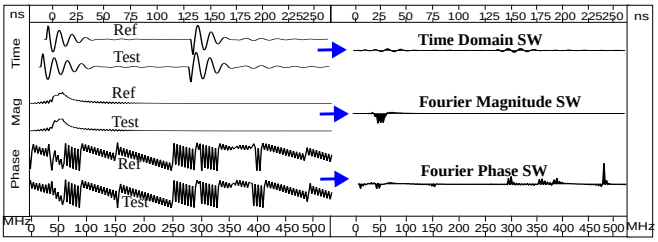

Figure 4. Time and Frequency Domain Signature Waveforms.

the Time Domain Signature Waveform shown along the top right of the figure. In a similar way, the frequency components (both Fourier Magnitude and Fourier Phase) computed by the DFT of the reference and test waveforms are used to create the frequency domain SWs as shown in middle and bottom left of the figure. An "adjustment" is additionally performed on the Phase SW values to make them relative to the reference (see [2] for details). Both the time and frequency domain SWs are shown shaded to a zero baseline. The sum of the absolute value of the areas corresponding to the shaded regions in a SW is called a Signature Waveform Area (SWA). SWAs are used in the regression analysis procedure for TSA.

3.3 Linear Regression Analysis

Linear regression is used to "track" signal variations caused by process and technology-related variation effects. The procedure is simple and is based on the analysis of scatter plots. The analysis can be performed on any of the three SW representations; Time domain, Fourier Magnitude (FM) or Fourier Phase (FP), shown in Figure 4.

As an illustrative example, Figure 5 shows two columns of FP SWs obtained from supply pads Vdd_x and Vdd_y from eight simulation experiments of a test device (not shown). The same input sequence was used in the 8 simulation experiments. The first simulation experiment was performed on the defect-free nominal device and its results were used to generate the seven pairs of Phase SWs shown in the figure. The pairs of SWs in the top 6 rows correspond to simulations on circuit models in which the transistor mobilities (μ_0) were varied globally by the amounts shown in the figure. The SWs from these simulations capture the signal variations produced under these simple Process Models (PMs) of the circuit. The last row shows the SWs from a bridging experiment. The model used in this "faulted" simulation is identical to the model used in the reference except for the presence of the defect.

The SW pairs in the first 6 rows are correlated. In other words, the magnitudes of the variations in the SWs of one row are (nearly) proportional to corresponding SWs in other rows. The SWAs shown on the far right and far left in the figure capture this correlation. For example, the ratio of the SWAs for Vdd_x and Vdd_y under PM#1 is 40/45=0.89 while those under PM#2 and 3 are 83/90=0.92 and 200/220=0.91. The Scatter Plot in Figure 6 plots the SWAs of Vdd_x (x-axis) against the SWAs of Vdd_y (y-axis) and illustrates that the SWAs PMs #1 through #6 track linearly. The phase shifts caused by global process variations are correlated across the supply ports of a device. The regression line shown in the figure is the "best" approximation of the SWA ratios (under the least squares criteria). The shaded region around the regression line is labeled as the Process Variation Zone (PVZ) and is delimited by 3σ prediction limits. The Process Variation Zone accounts for small variations in the SWA ratios caused by instrumentation error, measurement noise and intra-device process variations.

In contrast, the ratio of the SWs labeled G along the bottom of Figure 5 is not closely approximated by the same ratio that characterizes the SWs of the process models. The defect introduces significant regional variation in the SW of

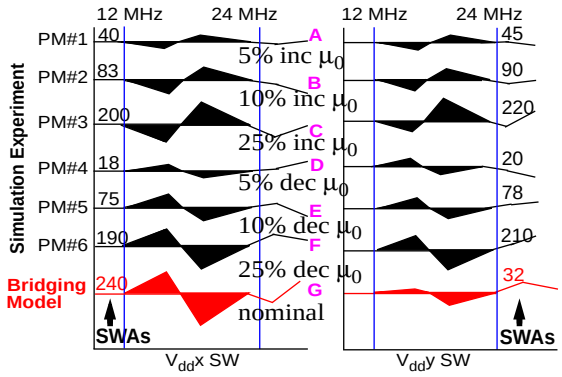

Figure 5. Vdd_x and Vdd_y Fourier Phase (FP) Signature Waveforms from 8 simulation experiments.

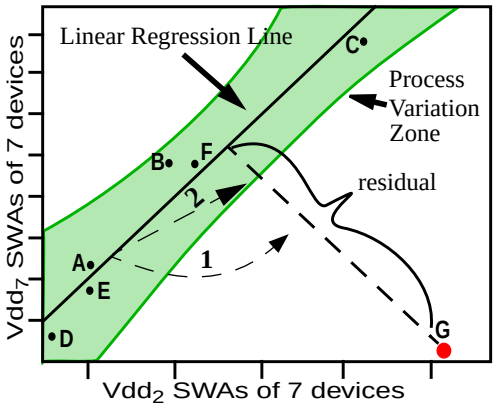

Figure 6. Scatter Plot, Regression Line and prediction limits (PVZ) using data from Figure 5.

Vdd_x due to its proximity to this supply port. In contrast, the RC components of the supply grid attenuate the signal at the more distant Vdd_y supply port. The ratio of SWAs under these conditions is given by 240/32=7.50. In this case, the ratio is large enough to allow the corresponding data point in the scatter plot to be identified as an outlier, as illustrated in Figure 6.

The standard statistical method of analyzing variance in scatter plots is through residuals. A residual is defined to be the shortest distance from a data point (see point G in Figure 6) to the regression line. Residual analysis, used in combination with the 3σ prediction limits, makes it straightforward to decide the pass/fail status of a device for a pair of supply port measurements. If more than two supply port measurements are analyzed, a test device passes if it produces residuals under all pairings that are within the PVZs of the corresponding scatter plots. In contrast, a defective device is expected to produce at least one data point outside these zones.

Section 3.1 described a second source of correlation that relates path delays and Fourier phase in I_{DDT} transients. This relationship and the RC attenuation characteristics of the supply grid provide a means of monitoring path delays within a region of the device.

It should be noted that, although the analysis given in Section 3.1 was based on I_{DDT}, the same properties hold for V_{DDT} signals if certain conditions are met. V_{DDT} transients are related to the I_{DDT} transients though the RLC network characterizing the power delivery system in the test environment (see [14] for an example of such a system). Therefore, the transformation from I_{DDT} to V_{DDT} is through a set of linear system components. If the values of these components remain relatively constant across tests of the DUTs, then similar results can be expected under either analysis. The main advantage using V_{DDT} signals is that they can be measured "non-invasively" using high resolution voltage sampling instrumentation. This is an attractive feature in a production test environment, particularly given the usual space limitations in and around the test head and wafer handling system.

4.0 Experiment Setup

The focus of this work is to evaluate the sensitivity of TSA to delay-oriented defects. In order to determine this sensitivity, a set of simulations were conducted on circuit models in which the value of shorting and open defect resistance is varied with and without variations in circuit component parameters representing process variations. For each modeled defect, simulation experiments were performed on (1) a set of defect-free process models, (2) a set of faulted models across a range of defect resistances and, (3) a set of faulted models combining variations in both circuit components and defect resistance.

Table 1 list the experiments that were performed for the five inserted defects. For example, the second column indicates that five defect-free "nominal circuit" simulations were run (one for each inserted defect). Column three indicates that fifteen additional simulations were run on the defect-free circuit model, each under a different process model. Eleven of these process models included variations in only one parameter while the remaining four varied all nine modeled parameters over the range of +/- 25% of the nominal values. Columns four and five give the set of resistances modeled for each shorting and open defect, respectively. Column six lists the simulations performed using the combined models.

The simulation experiments were conducted on a full-custom design of an 8-bit 2's complement multiplier. A block diagram of this device is shown in Figure 7. The power supply pads for the core logic are labeled as V_{DD1} through $V_{DD8.}$ The locations of the defects reported on in this paper are shown in the figure, along with the general directions of signal propagation. The five test sequences

	Reference Runs	Process Runs	Nominal Shorting Faulted Runs	Nominal Open Faulted Runs	Faulted + Process Runs
Experiments	BR1-3, OP1-2	BR1-3, OP1-2	BR1-3	OP1-2	BR1-3, OP1-2
# of models	1	15	12	12	3
Total # of sims	5	75	36	24	60
Resistances or Transistor/Circuit parameters varied by +/– 5%, 10% and 25%	None	μ_0, V_t, poly Ω, metal2 contact Ω, metal cap. over p-/n-well, p-/n-diff Ω, metal1 contact Ω, poly cap. to substrate, metal1 to metal2 cap.	50K, 25K, 20K, 15K, 12K, 10K, 9K, 8K, 7K, 6K, 5K, 2K, 1K, 100 and 50. (Ω)	50, 100, 200, 500, 1K, 2K, 5K, 8K, 9K, 10K, 12K, 15K, 20K, 25K, 50K, 100K, 500K and 1M. (Ω)	4 selected resistances * 3 process runs varying all 9 parameters as shown in column 3.
# of circuit params varied per model.	None	1 (11 models). 9 (4 models).	None	None	9 (3 models).

Table 1: Simulation Experiments and Models.

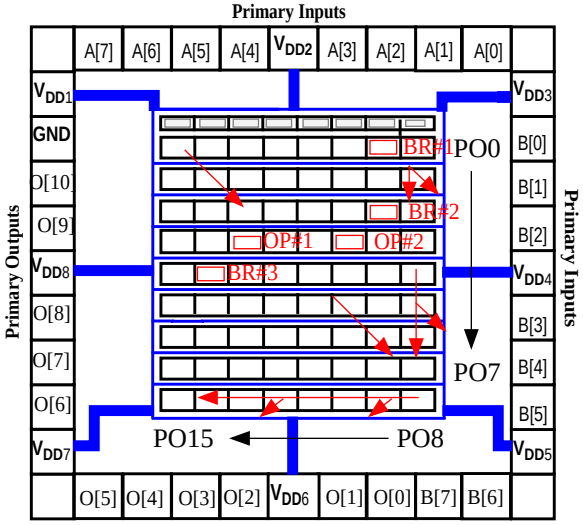

Figure 7. The layout of the 8-bit multiplier.

were run at 20 MHz for a duration of 150ns. The SPACE extraction tool [16] was used to extract the models from the layout using the TSMC 0.25 um technology parameters.

5.0 Experimental Results

The main objective of this work is to evaluate the sensitivity of TSA to the additional delay introduced by shorting and open defects. In the first section, a detailed analysis of path delays and Fourier phase is presented using a set of defect-free and bridging defective device models. Section 5.2 focuses only on the analysis of phase SWA scatter plots for other shorting and open defective device simulation experiments.

5.1 Delay Fault Phase Analysis

In Section 3.1, the analysis of path delays and Fourier phase indicated that the two are correlated across simulations of defect-free process models. In addition to showing that this relationship continues to hold in the multiplier circuit, simulations of a defective version are used to demonstrate that changes in path delays caused by a shorting defect produce regional uncorrelated phase shifts. Moreover, the pattern in phase behavior is consistent with the magnitude of the additional delay introduced by the defect, as given by the delay-phase relationship in defect free device models

Figure 8 shows a plot of the data obtained for the first bridging experiment. The x-axis of the graph displays the relative change in delay in the test model with respect to the nominal (at 0.0) along the longest path sensitized under the test sequence. These values are plotted against the Phase SWAs obtained from one of the supply pads. The data points from simulations of the defect-free process models are shown along the bottom of the figure. The circuit component variations in these models produce delay variations over the range of -2.0ns to 2.2ns. The 3σ prediction limits and regression line are labeled in the figure.

Figure 8 also shows the data points derived from a set of bridging defective simulation models, in which the resistance of the bridge was varied over a range of 50K to 5K. A few representative points are labeled in the figure along the left-most arc. These experiments were repeated under a selected number of process models. For example, the label "50KΩ + process" identifies one of these four curves given in the figure.

The parabolic shape of the left-most arc indicates that the phase shift is not linear with the magnitude of the additional delay introduced by the defect. The phase vs. delay plots of the other two bridging experiments reported in Section 5.2 are also characterized by a non-linear curve. This complicates the mapping from phase shift to path delay, using, for example, the method outlined in Section 3.1. Interestingly, the relationship is nearly linear for the open

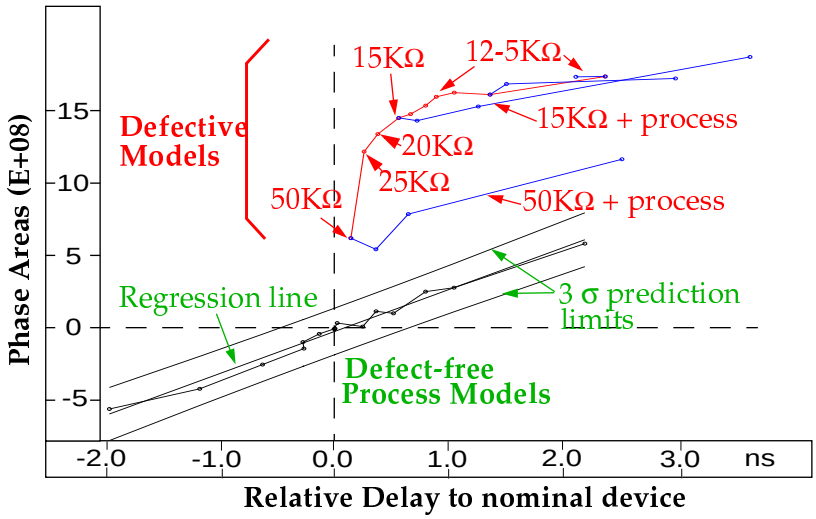

Figure 8. Phase SWA (y) vs. Relative delay (x) for defect-free devices (bottom) and shorting defective devices (top).

experiments.

It is also clear that phase is very sensitive to large values of the defect's resistance. For example, the defect in the 50KΩ model adds only 42 picoseconds of delay to the path but generates a large variation in the phase. Again, this is not the case for small values of resistance in the open experiments. Section 5.2 elaborates on these findings.

5.2 Scatter Plot Analysis of Defective Devices.

The results of three shorting and two open defective device experiments are presented in this section. The results indicate that it is possible to detect the additional delays introduced by shorting defects under any of the simulated values of defect resistance. For open defects, the task is more difficult but is possible for open resistance values that introduce significant additional delays.

The experimental results are presented in the form of scatter plots for the five experiments. Since the number of "faulted" simulations is large enough to clutter the scatter plots, in most cases, two scatter plots are shown. All scatter plots contain the fifteen data points obtained under the (defect-free) process models (column three of Table 1). The first of the two scatter plots additionally displays the data points generated under the "nominal" faulted models (columns four or five in Table 1). The second displays data points generated under the faulted process models, for selected values of defect resistance (column six in Table 1). Since the actual values of the Fourier Phase (FP) SWAs is not important, scale values are not displayed in the scatter plots. The analysis is shown only for the V_{DD1} and V_{DD5} supply pads. The wide separation of these supply pads in the layout (see Figure 7) suggests that this pairing is a good choice for maximizing the observability of regional delay variations.

Figure 9 shows the scatter plot for the data points generated under the faulted nominal simulation models of Shorting Exp. #1. The test sequence for this experiment is designed to sensitize both defect-free paths and paths through the defect site. The faulted simulation model's data points are labeled 1 through 15 in the figure. For this experiment, a sample of the defect resistances and corresponding relative path delays (w.r.t. the path delays in the nominal defect-free device model) along the sensitized path terminating at PO 5 are given as follows:

Short	1	2	3	4	5	6	7
Ω	50K	25K	20K	15K	12K	10K	9K
ns	0.042	0.044	0.047	0.310	0.980	3.090	fail

Table 2: Delays for defective models: Figure 9.

The device produces the correct functional values for defect resistances down to and including 10KΩ. Defect resistances for points 8-15 cover the range 8K–50Ω. From Figure 9, data points 1 (50KΩ) through 7 (9KΩ) move progressively further away from the origin, data point 8 reverses the trend and data points 9-15 form a cluster very close to data point 4. From the previous analysis of defect-free process models, the trend in the movement of the data points away from the origin indicates a progressive increase in path delays. This trend is consistent with the actual increase in path delay introduced by the defect in these models. The displacement of the data points below the PVZ indicates that the paths affected by the defect are closer to V_{DD5} than V_{DD1} (which is verified by the direction of signal propagation as shown in Figure 7).

Figure 10 shows the scatter plot for the 50KΩ faulted simulations under four process models: the nominal and three models in which nine circuit parameters were varied as indicated in Table 1. The data points are numbered such that the amount of delay introduced by the variations in circuit parameters increases from 1 to 4. The delays are given

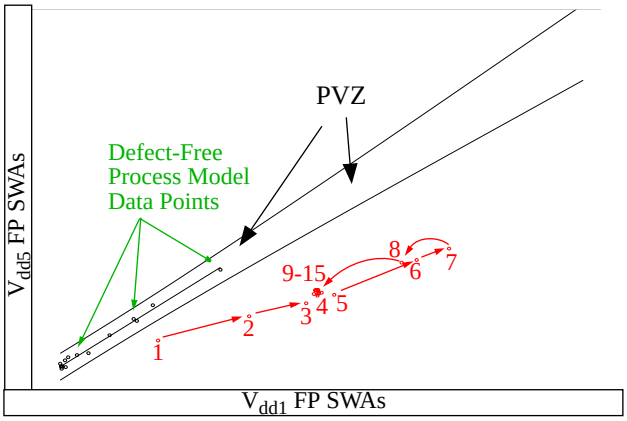

Figure 9. Shorting Exp. #1 V_{DD5} vs. V_{DD1} scatter plot for nominal process models.

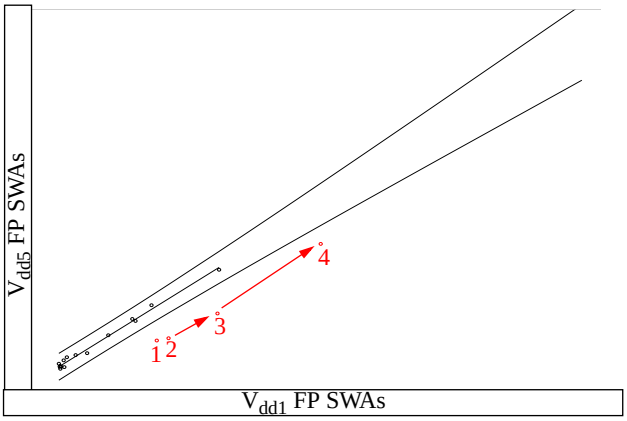

Figure 10. Shorting Exp. #1 V_{DD5} vs. V_{DD1} scatter plot for 50KΩ defect under 4 process models.

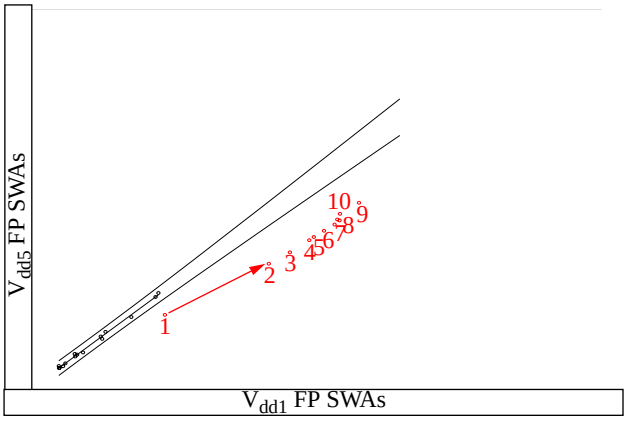

Figure 11. Shorting Exp. #2 V_{DD5} vs. V_{DD1} scatter plot for nominal process models.

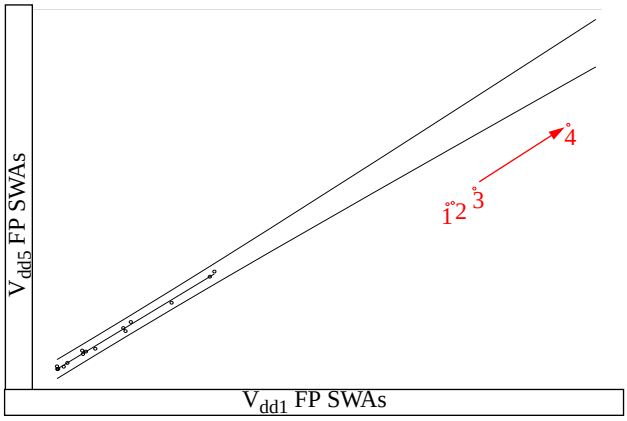

Figure 12. Shorting Exp. #2 V_{DD5} vs. V_{DD1} scatter plot for 15KΩ defect under 4 process models.

in Table 3.

2As expected, a line projected along these points is nearly parallel to the regression line. The fact that both the SWAs increase as delay increases indicates that phase tracks the delay introduced by variations in circuit component values as well as the delay introduced by the defect.

50KΩ Short	1	2	3	4
Sim	nominal	Combo 1	Combo 2	Combo 3
ns	0.042	0.167	0.363	1.660

Table 3: Delays for defective models: Figure 10.

Figures 11 and 12 show a similar set of results for Shorting Exp. #2. The test sequence sensitizes paths through the defect site to POs 6 and 7. All path segments beyond the placement of the defect (as shown in Figure 7) are affected by the defect. The correspondence of the numbers in the figure and defect resistances, as given in Table 1 are 1 (50KΩ) through 10 (5KΩ), respectively. The device failed functionally at 5KΩ in this experiment. The delays to PO 6 for the first seven defect resistances are given in Table 4.

Once again, the position of the data points tracks the delay added by the defect. Figure 12 shows the scatter plot for the 15KΩ faulted simulations under four process models. Similar conclusions can be drawn from these results as were given for Shorting Exp. #1.

Short	1	2	3	4	5	6	7
Ω	50K	25K	20K	15K	10K	8K	6K
ns	0.126	0.245	0.369	0.558	0.799	1.06	2.42

Table 4: Delays for defective models: Figure 11.

Figures 13 and 14 display the scatter plots for Open Exp. #1. Similar to Shorting Exp. #2, the test sequence propagates transitions through the defect site only. There are no defect-free paths sensitized under this test sequence, other than the path segments leading to the defect site. The sensitized path under analysis terminates at PO 8.

The correspondence of the numbers in the figure and

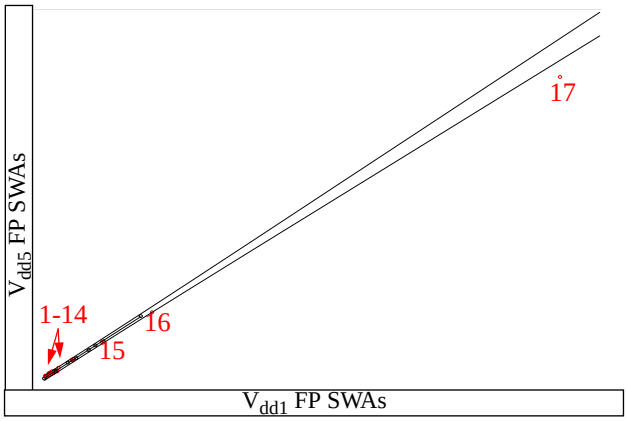

Figure 13. Open Exp. #1 V_{DD5} vs. V_{DD1} scatter plot for nominal process models.

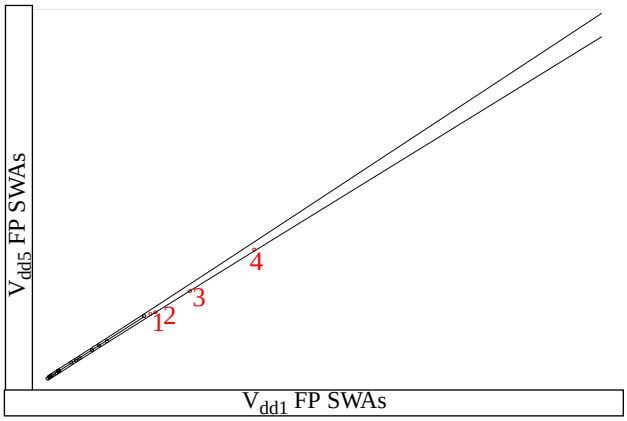

Figure 14. Open Exp. #1 V_{DD5} vs. V_{DD1} scatter plot for 100KΩ defect under 4 process models.

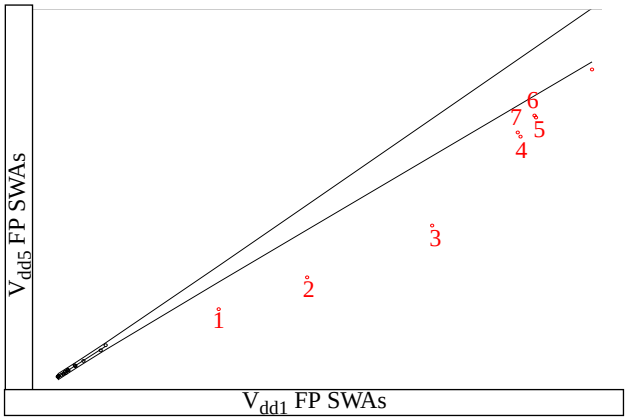

Figure 15. Shorting Exp. #3 V_{DD5} vs. V_{DD1} scatter plot for nominal process models.

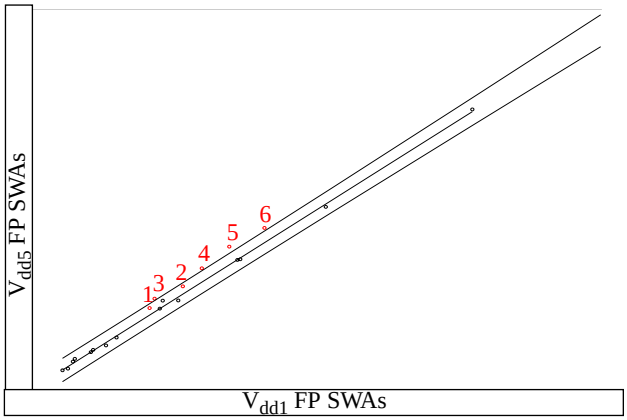

Figure 16. Open Exp. #2 V_{DD5} vs. V_{DD1} scatter plot for nominal process models.

defect resistances, as given in Table 1 are 1 (50Ω) through 17 (500KΩ), respectively. The device did not fail functionally at any of these resistance values but did under one of the faulted process models. The delays to PO 8 under a selected set of open resistances are given in Table 5.

As shown in the scatter plot of Figure 13, only data

Open	10	12	13	14	15	16	17
Ω	10K	15K	20K	25K	50K	100K	500K
ns	0.146	0.228	0.310	0.396	0.791	1.530	6.770

Table 5: Delays for defective models: Figure 13.

point 17 (500KΩ) falls outside of the PVZ. Data point 16 (100KΩ) is located on the lower prediction limit in a region of the PVZ, but is further removed from the origin than the data point generated under the worst-case (slowest) process model. The delays introduced by the other values of the resistance are not detectable as delay faults. For example, data point 15 (50K) is located within the PVZ.

Figure 14 shows the results of simulation runs on the 100KΩ open defective model. Although the data points fall within the PVZ, they do so outside the region containing the data points generated under the defect-free process models. Note that with a more restricted process skew tolerance, relatively low resistive opens such as these could be identified as outliers.

Figure 15 and 16 show the scatter plots of the faulted nominal simulation models for Shorting Exp. #3 and Open Exp. #2. Although the details are omitted, similar conclusions can be drawn concerning the trends in the (labeled) data points generated under these faulted models.

6.0 Conclusions

The analytical framework that describes the basis of the TSA regression model, e.g., the relationship between path delay and V_{DDT} Fourier phase, is presented in this paper.

In addition, simulation results demonstrate that TSA is able to detect the regional delay variations caused by shorting and open defects through regression analysis of phase scatter plots. In this analysis, the phase shifts in the fre-

quency components of two V_{DDT} supply pad signals were found to be well correlated in defect-free device process models. For the shorting defective device models, phase shift regression analysis could be used to distinguish between the regional delay variations introduced by defects and the global delay variations introduced by process for any of the simulated values of defect resistance. This was not possible for smaller simulated values of open defect resistance. Further restrictions on the region defining process tolerance in the TSA regression model and cross-vector regression analysis are under investigation as a means of improving the delay fault detection capabilities of TSA for open defects.

For shorting defects, increases in the path delay caused by decreasing the defect's resistance introduced increasing amounts of regional delay variation. The trend in the movement of the scatter plot's data points for models incorporating decreasing values of resistance followed a trajectory similar to that shown by arc 1 in Figure 6. In this case, it is not possible to predict the magnitude of the additional delay using the same technique demonstrated for delays introduced by process variations [2]. In contrast, the trend in the movement of the data points of models incorporating increasing values of open resistance remained linear, similar to that exemplified by line 2 in Figure 6. In general, shorting defects are more easily detected than open defects because they introduce a more pronounced regional phase shift in the V_{DDT} signals of the device.

Overall, these results suggest that TSA is a promising technique that could provide unique defect-detection capabilities in a production test suite.

Acknowledgments

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