Defect Detection using Power Supply Transient Signal Analysis

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Abstract

Transient Signal Analysis is a digital device testing method that is based on the analysis of voltage transients at multiple test points. The power supply transient signals of an 8-bit multiplier are analyzed using both hardware and simulations experiments. The small signal variations generated at these test points are analyzed in both the time and frequency domain. A simple statistical procedure is presented that captures the variation introduced by defects while attenuating those variations introduced by process variations. The results of the analysis show that it is possible to distinguish between defect-free and defective devices in both simulations and hardware.

1.0 Introduction

Transient Signal Analysis (TSA) is a parametric approach to testing digital integrated circuits [1][2]. In TSA, defect detection is accomplished by analyzing the transient signals measured at multiple test points of a device. The approach offers two distinct advantages over other logic and parametric testing methods. First, device coupling mechanisms (i.e. power supply) permit the detection of defects at test points that are not directly affected by the defect. Consequently, error observability is greatly enhanced in TSA since they need not be propagated to primary outputs. Second, by cross-correlating the data sampled from multiple test points, false detects caused by mistaking signal variations resulting from process drift as signal variations resulting from defects, are reduced. In fact, all useful parametric test methods must address this problem. The proposed technique works because the effects of process drift tend to be global, changing circuit parameters uniformly across the entire die (or very large portions of it). Hence, the corresponding change in the transient response of the device produces signal variations that are correlated at all test points on the die. In contrast, signal variations caused by a defect tend to be regional with larger amplitudes at test points closer to the defect site. This results in a change in the cross-correlation profile. The RC attenuation effects of the device coupling mechanisms reduce the amplitude of the variation as a function of distance from the defect site.

A simple statistical method is presented that is effective in attenuating the signal variations that are correlated (those caused by changes in the process) with respect to those that are regional (those caused by defects). The absence of correlation in one or more test point signals is used to identify defective devices.

In previous work, the analysis was carried out using the transient signals measured on core logic test pads on the outputs of logic nodes [3]. Core logic test pads are contact opens in the passivation layer to metal below. Although this strategy is sensitive to both logic faults and parametric defects that cause changes in propagation delay, several disadvantages are also evident. For example, the additional capacitive load introduced by the core logic test pads degrades circuit performance. Assuming that the supply rails are the primary coupling mechanism [4], power supply test points are more sensitive to signal variations introduced by defects and less intrusive than points in the core logic.

In this paper, experiments are designed to determine the effectiveness of analyzing power supply transient signals as a means of identifying defective devices. Multiple versions of an 8-bit multiplier were fabricated and simulated with bridging and open defects. The results show that it is possible to detect these defects while compensating for injected process variation.

The rest of this paper is organized as follows. Section 2.0 outlines some related work. Section 3.0 describes the TSA method. Section 4.0 presents the experimental setup for both the hardware and simulation experiments, Section 5.0 presents experimental results and, finally, Section 6.0 summarizes our conclusions and areas for future investigation.

2.0 Background

Parametric device testing strategies are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of quiescent supply current or transient response [5]. Many types of parametric tests have been proposed [6] but recent research interest has focused on two types I_{DDQ} [7] and I_{DD} [8].

I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value.

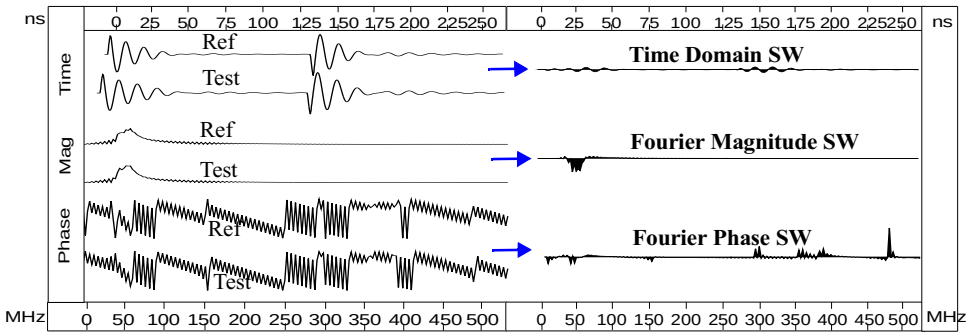

Figure 1. Time and Frequency Domain Signature Waveforms.

I_{DDQ} has been shown to be an effective detection technique for CMOS bridging defects, but is not applicable to all types of CMOS defects [9]. Furthermore, the near-future effectiveness of IDDQ as a defect screen has been questioned because defect currents may be difficult to resolve within the high background leakage of large deep submicron devices (<0.15microns) [10].

Several dynamic supply current I_{DD}-based approaches have since been proposed to overcome the limitations caused by the static nature of the I_{DDQ} test [11][12][13][14][15]. In general, these I_{DD}-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as I_{DDQ}, however they do not provide a means of accounting for process tolerances and are therefore subject to yield loss.

Recent related works, show promising results and are based in principle on the process calibration technique that we have proposed [16] and [17]. However, calibration is performed in these techniques across test sequences rather than within a single test sequence. Although these methods are simpler to implement since only one waveform is analyzed per test sequence, it has yet to be determined which of these methods can be adapted to provide adequate defect sensitivities for large deep submicron devices. The multiple test point measurements taken in TSA enhances defect sensitivity at the expense of increased measurement and computational complexity.

3.0 TSA Method and Model

TSA identifies defective devices by cross-correlating the waveforms measured simultaneously at topologically distinct locations on the device as a test sequence is applied to the primary inputs. The coupling model of digital devices provides the mechanism and the cross-correlation of multiple test point waveforms provides the means by which TSA can distinguish between defect-free and defective devices. The power supply, internodal coupling capacitances, well coupling and substrate coupling create an RC network in a digital device which are the mechanisms by which signal variations at a logic node (e.g. due to the presence of a defect) induce signal variations at test points on the power supply. These variations are regional since the RC network attenuates them as a function of distance from the defective node. Therefore, the signals measured at multiple test points can be cross-correlated to detect a defect by analyzing the differences in signal magnitude and phase at the test points. However, signal variations also result from changes in fabrication process parameters, making it difficult to isolate the variations caused by defects. Thus, an important issue is to differentiate between variations due to defects versus those due to process drift. The inability to do so can result in yield loss. In previous work, we determined that signal variations caused by changes in the process tend to be global and measurable in all test point signals [1]. More importantly, the signal variations caused by process are proportional across the test points, making it possible to attenuate them using simple signal post-processing techniques. The cross-correlation technique described below is able to calibrate for variations caused by the process and significantly improve the defect sensitivity of the method.

3.1 Signature Waveforms

TSA is based on the analysis of signal differences between a defect-free reference device and a test device. Signature Waveforms (SWs) capture these differences. SWs are created by subtracting the waveform measured from some test point on the test device from the waveform measured from the same test point location on the reference device. An example is shown in Figure 1. The V_{DD} waveform from the reference (Ref) is shown along the top left plot while the V_{DD} waveform from a test device (Test) is shown below it. Subtracting the test waveform from the reference creates the Time Domain Signature Waveform shown along the top right of Figure 1. The SW is shown shaded to a zero baseline. This area corresponding to the shaded region is used in the statistical analysis to identify defective devices. The area under the curve, computed by evaluating the integral of the waveform using the trapezoidal rule formula over the time interval 0-250ns, is referred to as the Signature Waveform Area (SWA).

The effectiveness of the SWAs in capturing the signal

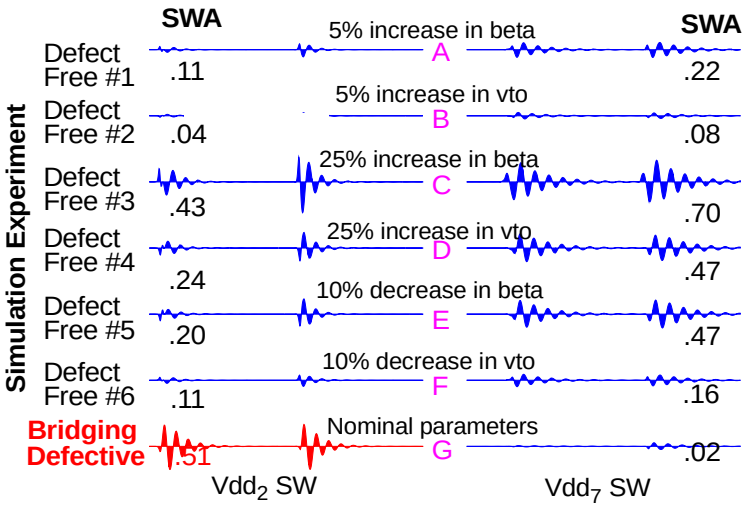

Figure 2. Vdd_2 and Vdd_7 Signature Waveforms from 7 simulation runs.

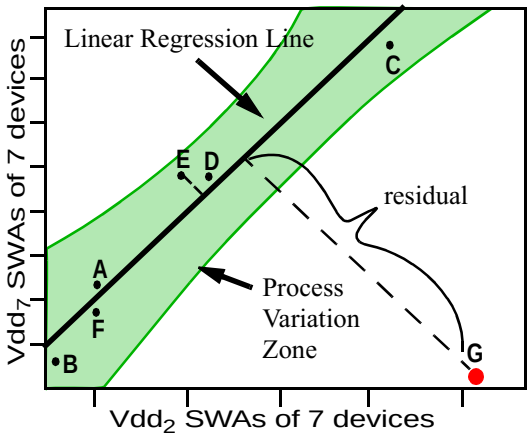

Figure 3. Scatter Plot, Regression Line and Confidence Band using data from Figure 2.

variations observable in the SWs is evaluated separately in the time and frequency domain. For the latter case, the raw time domain transient waveforms are used as input to a Discrete Fourier Transform (DFT). The frequency components (both Fourier Magnitude and Fourier Phase) computed by the DFT of the reference and test waveforms are used to create the frequency domain SWs as shown in middle and bottom left of Figure 1. The areas of the shaded portion of the Fourier Magnitude SW and Fourier Phase SW are used in the statistical analysis described below.

3.2 Pass/Fail Linear Regression Analysis

Linear regression is used to decide the pass/fail status of a test device. Using a set of SWs from simulations, Figures 2 and 3 illustrate the procedure and the properties exploited in TSA. Figure 2 shows two columns of SWs from two test points (Vdd_2 and Vdd_7). The pairs of SWs in the top 6 rows correspond to different simulation experiments designed to model simple changes in the process. These simulation experiments were performed on different models of the circuit in which exactly one of either beta or vto was varied globally from the nominal value by the amount shown in the figure. The last row shows the SWs from a bridging experiment. The model used in this "faulted" simulation is identical to the model used in the reference except for the presence of the defect. Other than these differences, all other parameters and conditions are identical for these simulations, including the test sequence.

The SW pairs in the first 6 rows are correlated. In other words, the magnitude of the variations in the SWs of one row is proportional to corresponding SWs in other rows. The SWAs shown on the far right and far left in the figure capture this correlation. For example, the SWAs for Vdd_2 and Vdd_7 in Defect-Free simulation experiment #1 are 0.11 and 0.22, respectively. These are proportional to the values 0.04 and 0.08, computed for Vdd_2 and Vdd_7 in Defect-Free simulation experiment #2. The Scatter Plot in Figure 3 plots the SWAs of Vdd_2 (x-axis) against the SWAs of Vdd_7 (y-axis) and illustrates that the SWAs from experiments 1 through 6 track linearly. Thus, a least squares estimate of a linear regression line (best fit line) shown in the figure tracks process variation in data points A through F. The shaded region around the regression line is called the Process Variation Zone and is delimited by a 99.9% (3σ) confidence band. The Process Variation Zone is wider than the data points it encloses and accounts for small non-linearity, measurement noise and intra-device process variations.

In contrast, the SWs labeled G shown along the bottom of Figure 2 are not proportional to the SWs in the other rows. In this case, the defect has produced regional variation in the SW of Vdd_2 due to its proximity to this supply rail. A much smaller amount of variation occurs in Vdd_7 due to the attenuation effect of the RC network. The lack of correlation in this pairing is illustrated by the outlier data point G in Figure 3. From the plot, it is clear that the behavior of this device is not characteristic to the norm defined by the regression bounds of the Defect-Free simulation experiments.

Based on this example, the pass/fail criterion under each test sequence is straightforward. Across all pairings of test points, if a test device generates a data point that falls outside of the Process Variation Zone for any pairing, the test device is defective. Although the same result was obtained for other pairing of test points in this experiment, this may not be the case for **all** test point pairings. This is the expected result since the variation generated by the defect is regional. Therefore, in the worst case, it may be necessary to analyze all pairing of test points in order to

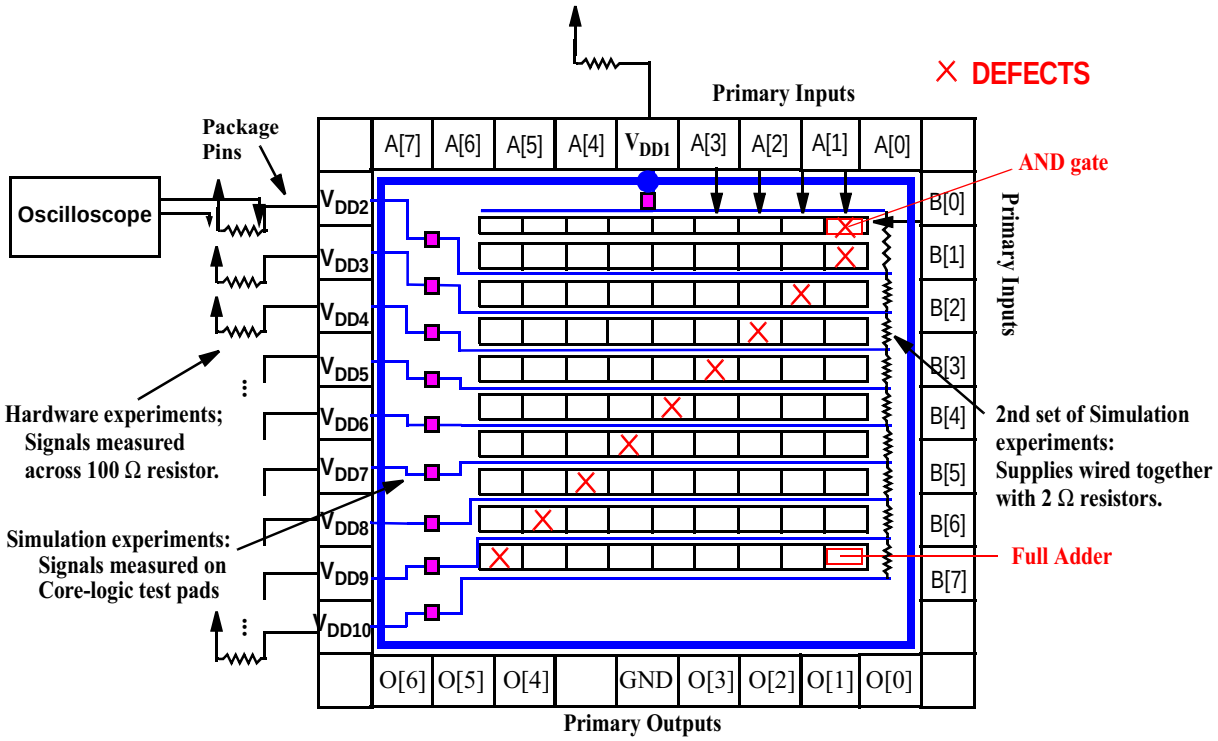

Figure 4. Block-level diagram of the multiplier showing the test point positions and defect locations.

determine if the test device passes under the test sequence. Ongoing research is designed to determine the minimal number of test point pairs that must be analyzed.

In general, the regression line itself is characterized by data points gathered from nominal defect free devices and those with parameters skewed at the limits of the particular process used. In this way, the regression fit accommodates good devices which operate at extreme, but valid, process specification corners.

3.2.1 The Decision Criterion

The distance labeled "residual" in Figure 3 is the metric on which the pass/fail criterion is based. A residual is defined as the shortest distance from the data point (G in the figure) to the regression line. A properly stimulated defective device is expected to produce at least one data point with a residual larger than the distance between the regression line and a chosen confidence band. It also follows that larger values provide greater confidence that the device is defective.

For the experiments in this paper, the 3σ confidence bands are used as the pass/fail threshold. Therefore, a test device fails if the residual is larger than 3σ for any test point pairing. In the analysis that follows, this is used to determine the effectiveness of the SWAs in capturing the signal variations introduced by defects.

4.0 Experiment Setup

TSA experiments were conducted on a full-custom design of an 8-bit 2's complement multiplier. A block diagram of this device is shown in Figure 4. The primary inputs, labeled A[0] through A[7] and B[0] through B[7] are shown along the top and right of the figure. Only six of the primary outputs are wired to the padframe (and observable at the package pins of the device.) The power supplies for the core logic are labeled as V_{DD1} through V_{DD10}. For the hardware experiments and one set of simulation experiments, the power supply is partitioned into 10 segments and wired out to 10 Vdd supply pins (no internal connection). A second set of simulation experiments were conducted with the supplies unified internally through a series connection of 2 Ω resistors (as shown on the right in the figure) to determine the impact of a unified supply on the detection sensitivity of the method. A 2 Ω resistance was used to simulate the supply grid configuration of a larger device.

Figure 4 also shows the test points used in the simulation and hardware experiments. For the hardware experiments, a difference waveform is computed using the signals measured on both sides of the 100 Ω resistors shown on the left in the figure. This is the most straightforward way of making these measurements and is representative of conducting TSA on packaged parts. As shown by others [16], a suitable alternative is to use a current probe if the series resistance value is difficult to determine or the IR voltage drop is problematic. Other experiments are underway to collect data from the core logic test pads (shown on the left in the figure), which is representative of conducting TSA at

Defect	Bridge#1	Bridge#2	Bridge#3	Bridge#4	Bridge#5	Bridge#6	Bridge#7	Bridge#8	Bridge#9
Resistance	**~0Ω**	**750Ω**	**~0Ω**	**50Ω**	**~0Ω**	**2.5KΩ**	**8.7KΩ**	**1.8KΩ**	**10KΩ**

Defect	Open#1	Open#2	Open#3	Open#4	Open#5	Open#6	Open#7	Open#8	Open#9
Resistance	**>100MΩ**	**6.75KΩ**	**>100MΩ**	**30.5KΩ**	**2KΩ**	**>100MΩ**	**>100MΩ**	**17KΩ**	**>100MΩ**

Table 1: Bridge and Opens resistance values in reference to Figure 5.

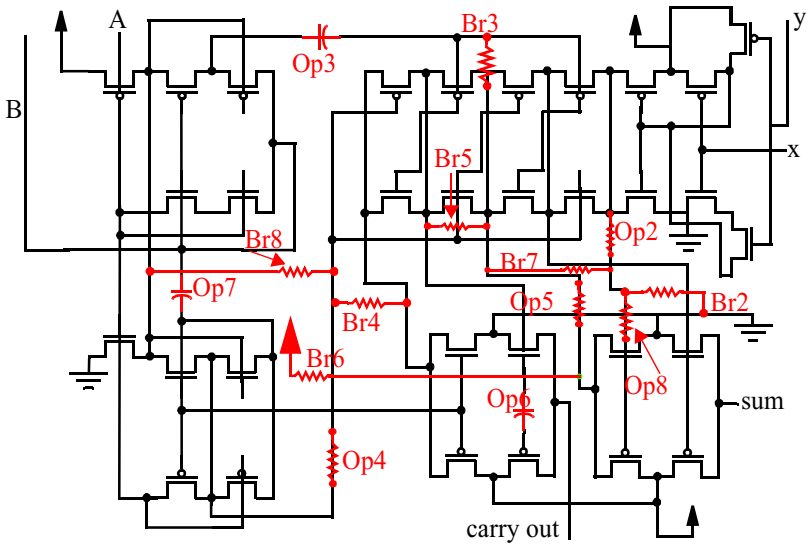

Figure 5. Schematic diagram of the AND gate (upper right) and transmission gate adder used in the multiplier.

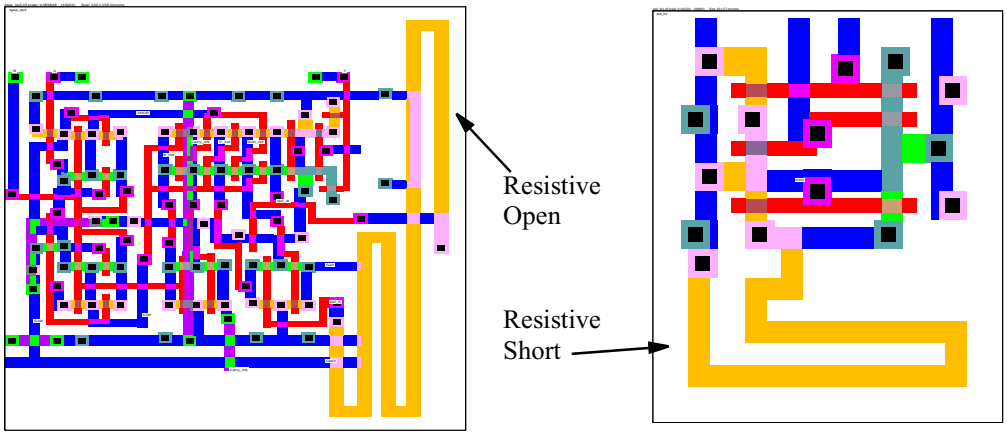

Figure 6. Transmission gate layout with resistive open (left) and AND gate with resistive short (right).

wafer probe. For the simulation experiments, signal measurements were made at both locations. However, signals from the core logic test pads are analyzed and reported on in this paper.

The input test sequences for the hardware experiments were run at 1 MHz. This was sufficient time for the signals to propagate through the circuit and allow the transient signals to decay and approach zero. It was not possible to run the simulation experiments at this frequency because the simulation time required to capture the data for both a rising and falling edge of the input sequence was too long (1us). Instead, the simulation experiments were run at 4 MHz for a duration of 250ns.

4.1 Defect Types and Locations

The regularity in the structure of the design made it possible to introduce defects at multiple locations while maintaining the ability to easily generate vector pairs which individually targeted a unique defect. The approximate

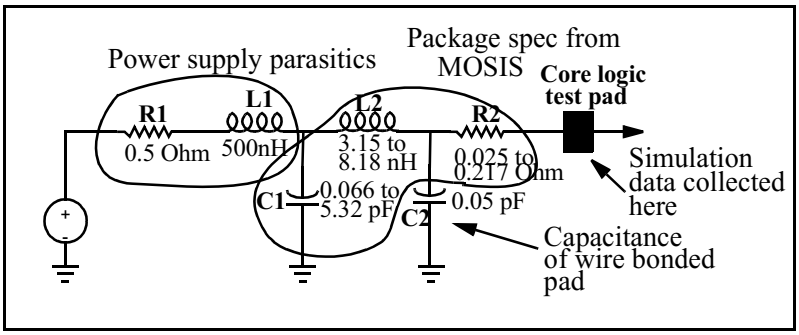

Figure 7. Package model used in Spice simulations.

	Reference Model	Defect-free Process Model	Defect-free Process Model	Defect-free Process Model	Defective Model
Bridging and Open Experiments	1-9	1-3	4-6	7-9	1-9
Number of models	1	30	36	10	2
Number of simulations	18	180	216	60	18
Transistor/Circuit parameters varied by +/-5%, +/-10% and +/-25%	None	trans. beta threshold voltage poly res. metal2 contact res. metal cap. over p-/n-well	trans. beta threshold voltage p-/n-diffusion res. metal1 contact res. poly cap. to substrate metal1 to metal2 cap.	All 9 parameters.	None
Number of circuit parameters varied per model.	None	1	1	9 randomly varied.	None

Table 2: Simulation Experiments and Models

locations of the defects are shown as 'X's in Figure 4.

Three versions of the multiplier were designed: a defect-free version, a version with 9 inserted shorts and a version with 9 inserted open defects. The resistance of the shorting defects in the bridging defective circuit varies between 0 Ω (hard short) and 10 KΩ. For the open defective multiplier, the range is 100 MΩ (hard open) and 2 KΩ. Table 1 gives the resistance values with reference to the labels of Figure 5. Figure 5 shows a schematic diagram of a full adder used for many of the cells in Figure 4. 14 of the 18 defects were introduced into 14 separate instances of this cell. Figure 6 shows a layout of the full adder (right) with a resistive open defect implemented using a long segment of p-diffusion for Open Experiment 2. The right side of Figure 6 shows the layout of a AND gate with a resistive bridge in p-diffusion for Bridging Experiment 1.

4.2 Experiment Description

For the hardware experiments, 4 devices of each version were fabricated for a total of 12 devices. The 4 defect-free devices and one set (4 devices) of either the bridging or open defective devices was used in each experiment. 18 experiments were conducted, each dedicated to detecting exactly one of the 9 bridging or open defects.

Accurate circuit models for the simulation experiments were generated using the SPACE extraction tool [18]. The lot averaged circuit parameters reported by MOSIS for the hardware devices were used to derive the technology file used by SPACE. The package parasitics were modeled as shown in Figure 7.

A simulation run was made using a nominal defect-free simulation model and either a bridging or open defective simulation model for each of the 18 experiments. In addition, seventy-seven other simulation models were extracted from the layout and used to analyze the influence of process variations. In these models, one or more of the transistor and/or circuit parameters reported by MOSIS were varied by the amounts stated above.

Table 2 summarizes the simulation experiment models and runs. For example, in Bridging and Open Experiments 1-3 (column 3), models were extracted and simulated in which the transistor betas, transistor threshold voltages, polysilicon resistance, metal2 contact resistance and metal capacitance over p- and n-well were changed individually by plus and minus 5%, 10% and 25% of the nominal values, for a total of 180 simulations. For Bridging and Open Experiments 7-9, nine transistor and circuit parameters were varied randomly in each model over the range +/-25%

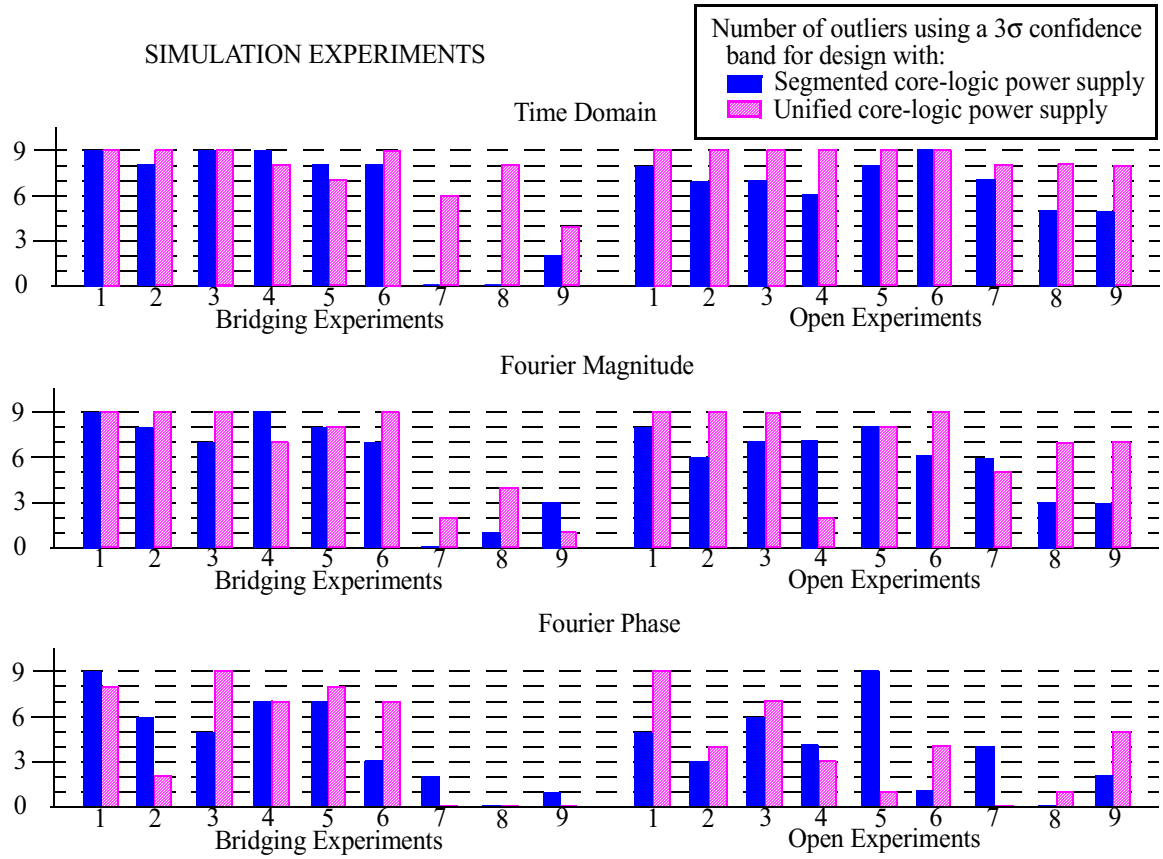

Figure 8. Time Domain, Fourier Magnitude and Fourier Phase Simulation Results.

of the nominal value to create ten simulation models. These models represent a worst case process scenario since it is likely that some of these parameters are dependent on others in a real process (e.g. beta and vto.)

5.0 Experimental Results

The analysis is performed using the Time Domain, Fourier Magnitude and Phase SWs obtained from 18 hardware and simulation experiments. Although the number of samples (test devices) considered in the hardware experiments differs from the number considered in the simulation experiments, the same waveform post-processing technique is applied to the data from both sets of experiments. For the hardware experiments, one of the defect-free devices was chosen as the reference device. For the simulation experiments, the data from simulations using the nominal transistor and circuit parameter model was used as the reference.

As shown in Figure 4, for each experiment, transient data was measured on each of the 10 supply rails simultaneously. Therefore, n*(n-1)/2 or 45 test point pairings are available for analysis. However, the results presented in the histograms shown in Figures 8 and 9 include only the 9 pairing involving Vdd_1 e.g. Vdd_1 and Vdd_2, Vdd_1 and Vdd_3, etc. Although these pairing sufficiently characterize the trend of the results for this device, it is recognized that the analysis of a larger subset of pairings may be required for larger devices.

Although the test circuit in these experiments is small, the success of this investigation is the demonstration that TSA can effectively detect defects and an indication that larger circuits can be handled. Since any degree of difficulty in detection can be compounded in large commercial circuits, frequent and easy detection of defects is a positive indicator. Because of limited hardware resources, simulation is used as the initial "acid-test" and can be manipulated to more completely explore and develop an optimal solution.

5.1 Simulation Results

The results of the simulation experiments are shown in Figure 8. As described in Section 4.2, 1 **reference** simulation and between **10 and 36 defect-free** simulations were run for each of the 18 Bridging and Open experiments. These were used to derive the regression lines and confidence bands for the 9 pairings of Vdd_1 with Vdd_2 through Vdd_{10}. A third simulation was run for each experiment using a model with a defect inserted.

The histograms of Figure 8 show the resulting number of "faulted" simulation data points which exceed the 3σ

limit. The solid bars correspond to the model in which the core-logic power supply is segmented (no internal connection) while the hatched bars show the results for the unified supply (joined internally using 2 Ω resistors as shown in Figure 4.) The Time Domain results are shown in the top histogram and the Frequency domain results are shown below it.

5.1.1 Unified Power Supply Results

The Time and Magnitude histograms indicate that all bad circuits are detected with the unified supply. However, in the Phase analysis, the defects in Bridging experiments 7 and 8 and Open experiment 7 were not detected. This degraded sensitivity is inconsistent with the previous hardware results [3] and the hardware results presented in this paper. It is probably due to weaknesses in the simulation model.

5.1.2 Segmented Power Supply Results

Under the segmented supply model, Bridging experiment 7 fails to detect the defect in the Time and Magnitude domains but is able to in the Phase domain. In general, the unified supply model yields better detection sensitivity than the segmented supply model, as is evident by the larger number of outliers across most experiments under the former. This may seem counter intuitive since a defect should cause large regional variations in the supply rail(s) to which it is directly connected and very little variation in disjoint supply rails. So, outlier data points should be easily generated for all pairings involving an affected rail and an unaffected rail. However, the segmented version is actually less sensitive because the confidence bands are much wider. This happens because the signals on each supply rail interact only through capacitive coupling mechanisms and are relatively independent of each other. This is in contrast to the direct (resistive) coupling of the unified supply. The direct coupling of the unified supply increases the correlation of signals across the die and "tightens" the data points from defect-free devices around the regression lines. Thus, the width of the confidence band is reduced and the sensitivity to outliers is increased. Although the multiplier is a very small circuit, this is a potentially important trend since most commercial designs use the unified supply model.

5.1.3 General Observations

The Time and Magnitude histograms of Figure 8 show nearly identical results. This is expected since the total areas under the curves are theoretically identical. However, here there is a slight difference because the area of only the first 200 harmonics of the frequency domain were computed. The analysis of specific frequency range(s) may be useful in enhancing defect sensitivity and is currently under investigation.

Both Bridging and Open Experiments 7, 8 and 9 show a notable decrease in the number of outliers. Closer inspection shows that the confidence bands for these experiments are wider than those computed for simulations experiments 1 through 6. This occurs because a fewer number of defect-free simulations were run (10) for experiments 7 through 9 than for experiments 1 through 6 (30 and 36). As the width of the confidence band is related to the number of samples as well as the dispersion in the data, a larger characterization set would probably improve the results for experiments 7-9 (although the defects were indeed detected anyway). In practice, it is important that a significant sample size (at least 30) is used.

The simulation experiments performed indicate that the Time and Magnitude analysis can identify defective devices without considering all 45 power supply cross correlations. Given a single reference supply (Vdd_1), fewer than 9 measurements were sufficient per circuit. Although the results are encouraging, it is difficult to definitively extrapolate the trend to large, more realistic sized circuits. One possibility is that more than one test point pairings will need to be considered because it is difficult to predict the effect of distance between the defect and the test points.

5.2 Hardware results

The limited number of defect-free hardware test devices (3 excluding the reference) did not permit the derivation of reasonable confidence bands for the data. Therefore, the confidence bands from the simulation experiments were used to compute the 3σ confidence bands for the hardware experiments. The approximation is a constant which is equivalent to approximating the hyperbolas defining the confidence bands in Figure 3 as straight lines. The residuals of the test devices were standardized (normalized) in both the hardware and simulation experiments in order to make this meaningful using

$$\frac{\text{residual}}{\sqrt{MSE}}$$

where MSE is defined as the sample variance of the defect-free residuals. The average width of the confidence band was computed in units of standardized residuals and used as an approximation of the 3σ confidence bands for the hardware experiments. The approximation is reasonable as long as the regression lines defined by the three defect-free devices in the hardware experiments (and those defined by the simulation experiments) are reasonable approximations of the true regression lines.

The hardware results are shown in Figure 9. The histograms are defined in a similar way to the simulation results. However, in these experiments, four defective devices were analyzed per experiment and the bars show the results computed for the defective device with the **minimum** number of outliers.

It is clear from Figure 9 that all 3 domains are effective

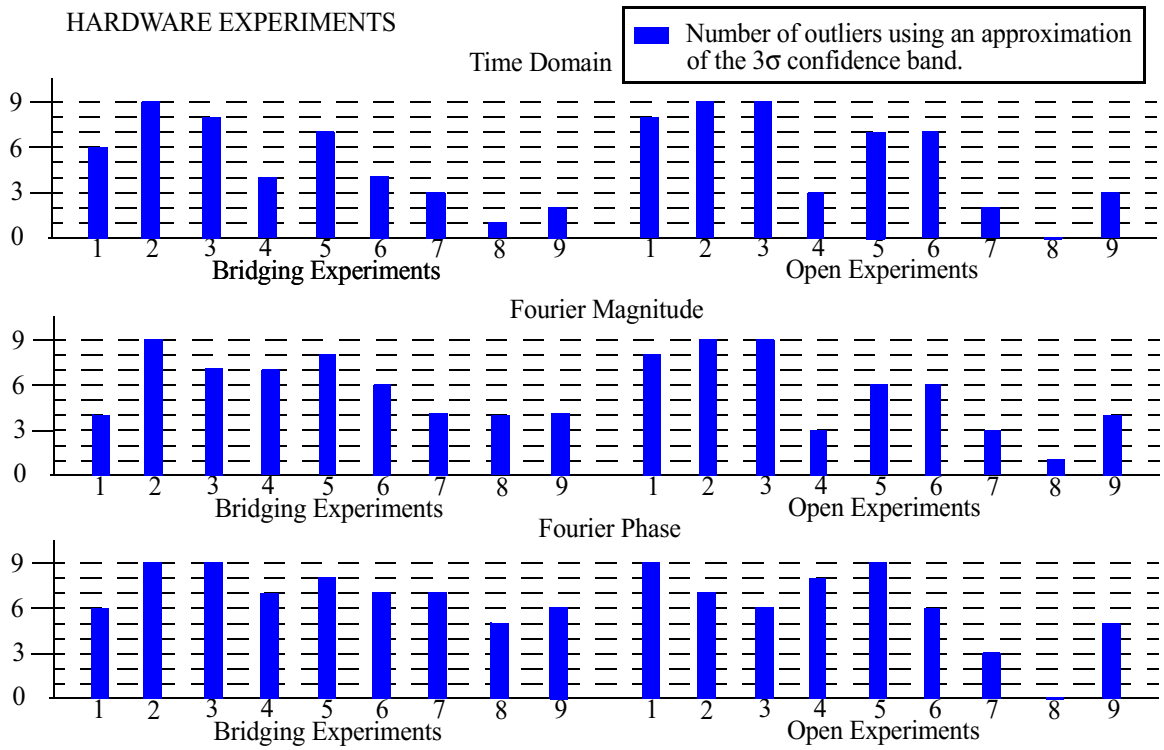

Figure 9. Time Domain, Fourier Magnitude and Fourier Phase Hardware Results.

in detecting defects. Again, the difficulty in passing open experiment 8 within the nine parings is probably due to the improperly characterized regression limits. However, all defects are covered if the remaining 36 Vdd pairings are considered. In addition, compared to the previous Phase Domain simulation results, the hardware Phase experiments show somewhat more frequent (thus easier) detection. This suggests that the simulation models used for Phase experiments need to be refined. Further improvements in the results for the Phase experiments are expected using measurements from the core-logic Vdd test pads (see Figure 4).

The high frequency of outliers across these experiments strongly indicate that proceeding to experiments using larger circuits is of value. In addition, as indicated in the previous sub-section, it is expected that the sensitivity of the metrics for the hardware experiments will tend to improve given a unified power grid.

Although the values obtained for the remaining three defective devices are not shown, they are similar to the results shown in Figure 9. This is expected since the defect causes a similar effect in each of the defective devices. This similarity also validates the results by reducing the probability that the outliers are the result of measurement error. The small differences in the results for the four devices are due primarily to measurement noise.

5.3 Discussion

Notable in these hardware and simulation experiments for both the unified and segmented supply models, is the high frequency of outliers across the experiments. This suggests that the analysis of fewer pairings may be sufficient to detect the defects in other designs. While it is difficult to claim that a single pair will be sufficient for large circuits, it is probable that the trend will persist and only a small set of pairs with perhaps a single reference point, is required. Further experiments are planned to investigate this aspect of the technique.

Also of significance is that all 3 domains detect the failed circuits with similar capability. The significance of this observation is that degrees of freedom are introduced into the methodology. That is, in a final implementation, one or all of the domains may be measured depending on their “defect sensitivity” and the practicality of the manufacturing solution. For instance, while each of these domains may, in fact, capture a specific characteristic of the circuit behavior, the relative performance of each domains to specific types of defects is unknown at this time. While it may be conjectured that each domain can target non-overlapping defect-types, the experimentation here is insufficient to judge this.

6.0 Conclusions

Transient Signal Analysis (TSA) is proposed as a means of identifying defects while compensating for process drift.

The voltage transients at the power supply pins (for segmented and unified power grids) are measured and processed in the time and frequency (magnitude and phase) domains. These waveforms are transformed into a SWA, which is the area of the difference waveform constructed using the sampled transients of a test and reference device. The set of regression lines from scatter plots of SWAs from different Vdd pins comprise a profile of the parametric operation of a device.

Using regression analysis, defect free data (perturbed by simulated process variation) is used to determine a correlation profile characteristic of a "good" device. For experimentation, a failed circuit deviates from this profile by more than 3σ. This method and criterion compensates for transient variations resulting from assumed process drift. This is a notable strength of the approach.

Simulation and hardware experiments were performed on an 8-bit multiplier to evaluate the effectiveness of the TSA procedure and its applicability to larger circuits. While it is difficult to prove that the current approach is directly transferable to realistic chips, the results do suggest that such investigation is not impractical. That is, it was shown that the injected defects were detectable using a small subset of the n^2 test point pairings. In addition, while the hardware fabricated possessed the unrealistic drawback of segmented power supplies, the positive results and trends remain valid overall because simulation suggests that the performance of the segmented supply model is pessimistic compared the to unified one.

The 3 domains explored provided similar defect detection capability but their relative effectiveness of targeting different defect types is yet unknown. However, the possibility of 3 alternatives to accomplish similar TSA tasks does offer flexibility in developing a practical production-oriented solution.

In the near future, improvements to the method will involve: minimizing the number of Vdd pairs cross correlated, investigation of self-relative measurements (which would eliminate the need for defect free references), experiments on real circuit products and formulation of a practical implementation/approximation of the TSA technique.

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