Measuring Within-Die Spatial Variation Profile through Power Supply Current Measurements

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ABSTRACT

Spatial variation in process parameters can have a significant impact on parametric yield of integrated circuits. We present a test structure and measurement technique for statistical characterization of process variation with programmable spatial granularity. The proposed structure can measure spatial variation at a desired level of granularity by controlling the leakage and on-current state in different spatial regions through input vectors and measuring the corresponding quiescent (I_{DDQ}) currents at power supply ports. This minimally invasive and low overhead variation measurement approach can be extended to measure spatial variation profiles in actual product chips by leveraging the existing power delivery architecture and power control circuits such as voltage islands and power gating. Measurements on a test chip fabricated in a 65 nm process show nearly a 100% leakage variation and 7% on-current variation over a 558 µm by 380 µm silicon area with nearly 3X chip-to-chip leakage variation.

1. INTRODUCTION

Technology scaling has led to a significant increase in process variability due to effects such as random dopant fluctuation and imperfections in lithographic patterning of small devices. These variations cause significant unpredictability in the power and performance characteristics of integrated circuits. Process variation is typically observed at several different scales such as lot-to-lot, wafer-to-wafer, within-wafer and within-field variation. Lot-to-lot and wafer-to-wafer variations are caused by long-term drifts in tools and wafer processing conditions. Within-wafer variation primarily occurs due to wafer-level non-uniformities such as post exposure bake (PEB) temperature gradient [1] and resist thickness variation [2]. Within-field variation, on the other hand, stems from optical sources such as across field focus and dose variation [3] and mask errors [4]. In addition to the above sources, within-die variation can also be caused by layout dependent systematic effects such as pitch and density dependent line-width variability [5] and microscopic etch loading [6]. The Lot-to-lot and wafer-to-wafer sources of variations are typically temporally correlated while the within-wafer and within-die components usually exhibit a significant amount of spatial correlation.

In this work, we present a test structure to measure spatial process variation profile. The structure can be used to estimate within die leakage and on-current variation due to spatial process gradients. A key feature of the proposed measurement technique is that it relies on I_{DDQ} current measurements of the chip. This feature makes the proposed structure quite attractive over traditional measurement circuits such as embedded ring oscillators [7, 8] and addressable MOS arrays [9]. The embedded ring oscillators are usually placed at multiple spatial locations and their frequencies can be measured to reflect spatial variation. The addressable MOS arrays can provide more detailed information than the ring oscillators at a very fine spatial granularity but require large tester overhead. Furthermore, these test structures require additional ports for measurements and essentially provide a point measurement in a spatial region of interest.

In our earlier work [10], we showed that the current measurements made at different power supply ports of the chip are strongly correlated to the magnitude of the leakage current in the spatial region near each of the individual power supply ports. This method is excellent in determining the intra-chip leakage variation map. However, the method proposed in [10] requires considerable tester and design resources for measuring the multiple supply pad currents. The circuit proposed in our current work overcomes these limitations by taking a single global quiescent (I_{DDQ}) current measurement. I_{DDQ} measurements are very robust in characterizing long-range spatial variations because they measure the aggregate effect in a spatial region and thus naturally eliminate local random and local layout dependent effects.

The other key feature of the structure is that it can be easily programmed to obtain desired level of spatial granularity during measurements. The programmability is achieved by controlling the input state of the devices in different spatial regions or islands. For example, we can control the leakage of a spatial region by putting the logic in the region in either low leakage (*sleep*) state or high leakage (*active*) state. This measurement technique is very effective in isolating the process characteristics of a spatial region. Furthermore, the technique can also be extended to characterize spatial variation profile in actual product chips where in-built power reduction techniques such as supply gating and multiple voltage islands can be exploited to expose within-die variation characteristics in global I_{DDQ} measurements.

The design of the structure and the detailed measurement results are discussed in the following sections. The proposed structure is used to characterize leakage and on-current variations in a variety of different sized spatial islands in a set of chips fabricated in a 65 nm process. The results show that the measured spatial variations have a random local component and a global deterministic component. Such information can be efficiently captured by the proposed characterization structure.

2. TEST STRUCTURE

Figure 1 shows the block diagram of the test structure. The structure contains an 80x50 array of test circuits (TCs). Each test-circuit in the array comprises of a pseudo test inverter with a pMOS and an nMOS device connected in series between V_{DD} and GND. The gate terminals of the pMOS and the nMOS devices in the pseudo inverter are independently controlled through scan flip flops. The scan flip flops of all test circuits are connected in a scan chain configuration. The current drawn by each logic inverter can be controlled by scanning an appropriate input pattern. For example, the test circuit can be switched into a low leakage state by turning off both the nMOS and the pMOS devices in the inverter or into a higher leakage state by enabling only the nMOS transistor. The circuit can also be switched into an on-current state by enabling both the nMOS and the pMOS transistors.

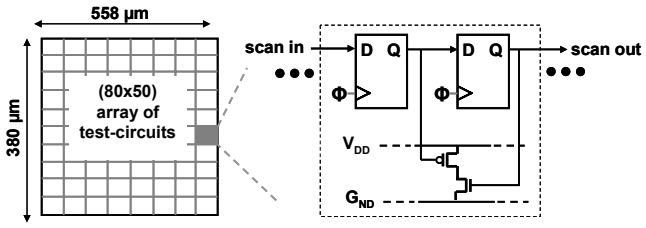

Fig 1: Block diagram of the test macro and schematic of one test circuit element

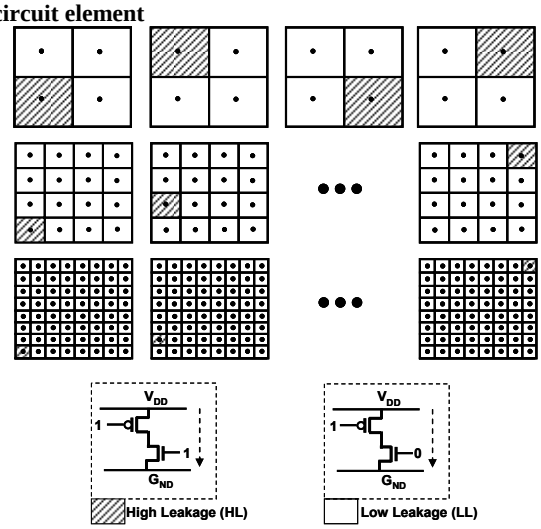

Fig 2: Spatial leakage patterns created by putting test circuits in different spatial islands of the array in high leakage state. Three cases with spatial granularity of 4, 16, and 64 partitions are considered.

The control structure of the test circuit shown in Figure 1 allows us to measure spatial variation in leakage and on-current with programmable granularity. For example, in order to obtain spatial leakage profile, the logic inverters in different islands of the array are configured into low leakage (LL) and high leakage (HL) states and a leakage current measurement is made through the global power supply. The LL state is configured by scanning a '10' into the FFs (disabling both the nMOS and pMOS devices in the inverter), while the HL state is configured by scanning an '11' (or '00') pattern, which disables the pMOS (nMOS) but enables the nMOS (pMOS). The size of the island determines the spatial resolution of the measurement. The average leakage characteristics of an island can be isolated by measuring the current with their TCs configured in the HL state and then subtracting the power supply current measured with the entire array configured in the LL state.

Figure 2 shows a block diagram view of the TC array for characterizing spatial leakage variation. The figure shows the set of HL islands investigated in three rows which we refer to as '4 islands' (top row), '16 islands' (middle row) and '64 islands' (bottom row). In the '4 island' analysis, the array is partitioned into 4 regions and configured such that three regions are placed in LL and one region in HL. For example, the upper left block diagram is configured such that the lower left island is in HL (shown shaded in the figure). The large number of devices configured in HL, i.e., 1000, in the 4 island experiments yields a coarse level of leakage characterization. The 16 and 64 island experiments incrementally improve on the leakage resolution by partitioning the array into more islands. This partitioning scheme allows us to measure spatial leakage variation profiles at 4, 16, and 64 island granularity through standard power supply quiescent current measurements.

We can perform similar experiments to characterize on-current variation. On-current characteristics of a spatial island can be isolated by configuring its TCs such that both nMOS and pMOS devices in the TCs are enabled ('01' pattern). However, the spatial coarseness of on-current measurements is constrained by the maximum acceptable current that can be supported by the power grid. In our experiments, we eliminate any IR drop issues by measuring a single TC on-current at a time. From these measurements, we can create the variation profiles for spatial granularities of 4, 16, and 64 partitions by summing the individual TC currents in the corresponding islands. The next section shows the measurement results for both leakage and on-current analysis.

3. EXPERIMENTAL RESULTS

The proposed structure was designed and fabricated in a 65-nm SOI process. We carried out experiments for both leakage and on-current variation on 33 copies of the test chip with different spatial granularities. For spatial leakage profile characterization, we first measured the current with the entire array configured in a LL state, and then again for each of the 84 (4+16+64) HL island configurations shown in Figure 2. After subtracting the LL current from each of the 84 HL currents, a within-die variation profile is constructed using a percentage change metric. The percentage change is computed by subtracting the current measured in a reference experiment from each of the currents measured under the remaining experiments in that group, i.e., either the 4, 16 or 64 island groups. For the within-die variation analysis, measurements made with the HL islands at the lower left corner of the array are used as the reference experiments. The percentage change numbers for each chip reflect the spatial leakage profile relative to the corresponding similar size lower left spatial region in the same chip. A similar metric is defined for representing the die-to-die variation. In this case, the reference is derived from a model which is constructed by distributing 250 µA of leakage current distributed uniformly across the entire array and divided by the number of islands used in the experiments. For e.g. in the 64 island experiments, the reference current is 3.9 µA (250 µA/64). This procedure normalizes the current measurements of all chips for a given island configuration by the same current value thus revealing the die-to-die variation along with the with-in die variation.

Figure 3 illustrates the within-die measurement results in 3D plots for three chips (rows) under each of the 4, 16 and 64 island configurations (columns). The (x,y) plane in the figure represent the center coordinates of each of the islands in the array, while the z-axis plots the percentage change. For example, the current profile surfaces for the 4 island experiments contain only 4 data points, one from each of the HL configurations along the top row of Figure 2. The current profiles for the 16 and 64 island experiments include 16 and 64 data points, respectively. The figures show that the magnitude of the within-die spatial variation in the 4 island results is smaller because of the averaging effect. The 4 island analysis does not capture the high spatial frequency variation in the leakage profile. As the number of partitions in the array is increased, the actual magnitude of the local variation in the leakage characteristics becomes more pronounced and higher spatial frequency

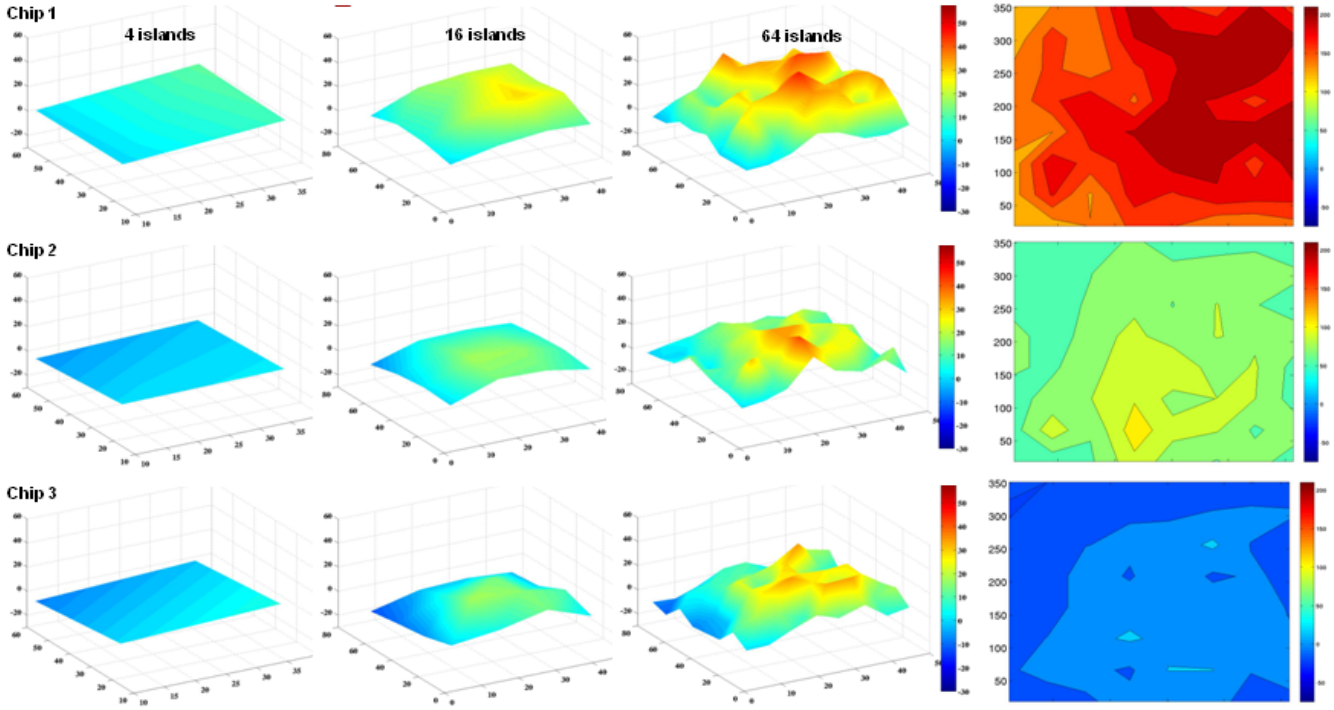

Fig 3: Measured within-die spatial leakage profile for three chips (top to bottom) with sleep island granularity of 4, 16, and, 64 islands (left to right)

Fig 4: Leakage profile (64 islands) for 3 chips with within-die and die-to-die variation

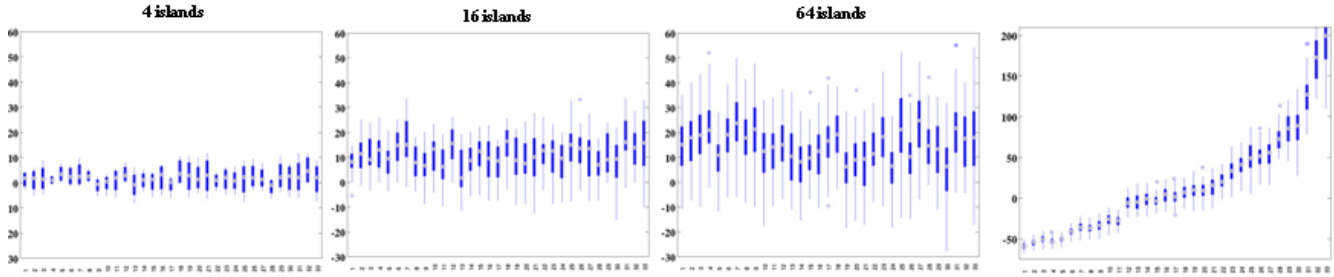

Fig 5: Measured within- die variation with 4, 16, and, 64 sleep islands for 33 chips. The range of variation increases with higher spatial granularity of islands.

Fig 6: Measured within-die and die-to-die variation (64 islands) for 33 chips

components are captured. Although the variation exhibits a large degree of randomness, a systematic component is also visible where leakage magnitudes are smaller along the edges particularly along the left edge of the array. This edge effect is evident in the 16 island analysis.

Figure 4 gives 2D contour views of the die-to-die profiles for these three chips under the 64 island experiments. In this case, all the currents in the three chips are normalized with respect to a common reference value. The difference in the overall magnitude of the chip-to-chip leakage characteristics is reflected in the bias of the contours to one specific region of the range. The variation within the contours reflects the within-die variation, with patterns similar to those described in reference to Figure 3. These contours show a significant die-to-die variation along with the within-die variation profile for each chip. It should be noted here that the chip wide global I_{DDQ} measurements can also provide mean die-to-die leakage variation information but unlike the results shown in Figure 4, the global I_{DDQ} measurement method does not provide any information regarding the spatial composition of the overall leakage of a chip.

Next we look at the leakage measurement data for all 33 chips. Figure 5 represents the within-die percentage variation data for 4, 16, and 64 islands cases in box plots. The box plots in Figure 5 provide a statistical perspective of the data, i.e., medium value, extreme values, etc., of the leakage variations across all 33 chips (x-axis). The chips are sorted according to their overall leakage characteristics, from low global I_{DDQ} (chip 1) to high global I_{DDQ} (chip 33). The increasing magnitude of the within-die spatial variation in the 16 and 64 island experiments is clearly evident. However, the within-die variability across the chips within each island group appears to be random and uncorrelated with the overall leakage current magnitude of the chip.

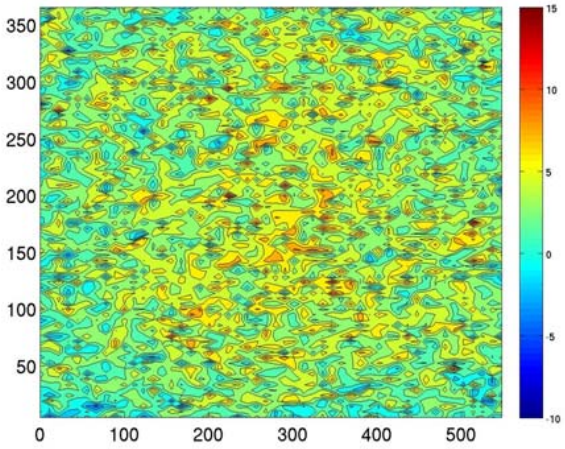

Fig 7: Measured within-die on-current variation. All 4000 TCs are measured individually with only one TC active at a time.

The box plot in Figure 6 is constructed using the die-to-die variation percentage change metric and the 64 island data. Once again, the chips are sorted in the increasing order of their total leakage. Here, it is more apparent that the level of variation is correlated with the overall leakage current magnitudes of the chip, i.e., higher leakage chips have larger levels of within-die spatial variation. From these figures, the range of within-die spatial variation is -30% to +60% while the range of die-to-die leakage variation is -75% to +210%, i.e., approximately 3 times larger over a set of 33 chips.

Next we look at the on-current measurement data. As mentioned in the previous section, we measure on TC at a time to avoid any voltage droop issues in the power grid. Figure 7 shows the on-current variation data for the 4000 test circuits from a measured chip. The figure shows that there is a systematic trend in the variation profile where the currents in the center appear to be higher than those at the edges. However, the spatial trend is not very clear due to superposition of the high frequency FET level random variation on top of the spatial profile. The total on-current variation includes both systematic and random components and spans from -10% to 15%.

The individual TC measurements shown in Figure 7 can be used to obtain spatial profiles for the 4, 16 and 64 island scenarios discussed previously for the leakage experiments. For example, the 64 island scenario is constructed by partitioning the array into 64 regions and summing the on-currents for all TCs in each spatial region. The total current value for each island is normalized with respect to the corresponding total current drawn by the lower left island. Figure 8 shows the on-current variation profiles for the 64, 16, and 4 island experiments. It is evident from the figure that as the spatial granularity becomes coarse, the spatial cut-off frequency is also reduced and higher frequency components such as FET level random variation is removed from the data.

The plot for the 64 island case shows a clear spatial trend in the measured data where the on-current magnitudes are smaller along the edges of the array. This trend is consistent with the corresponding leakage profiles shown in Figure 2. The total on-current variation range for the 64 island case is 7% as opposed to the 25% variation observed in the 4000 island case. The variation range

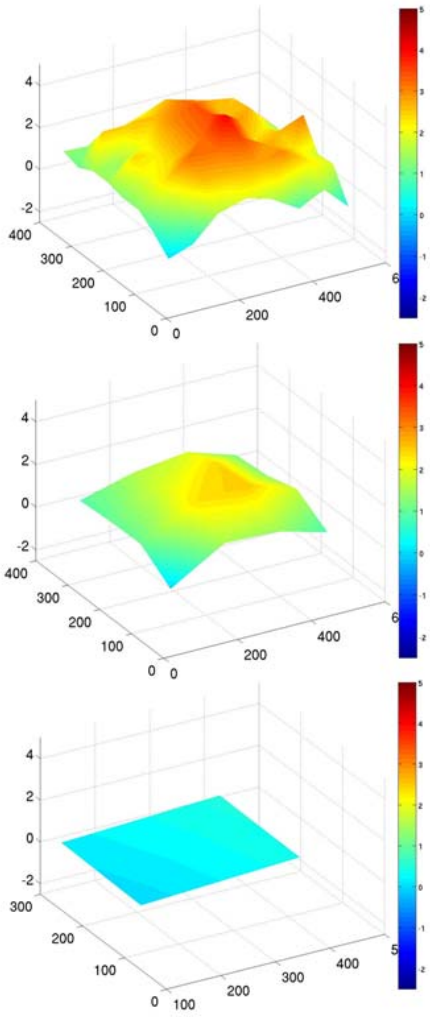

Fig 8: Measured within-die spatial on-current profile with sleep island granularity of 64, 16, and, 4 islands (top to bottom).

is further reduced for the 16 and 4 island scenarios due to the averaging effect with the 4 island case being too coarse to accurately capture the inherent spatial variation in the chip.

4. CONCLUSION

In this work, we presented a novel test structure that enables leakage and on-current variation to be analyzed at various levels of spatial granularity. The test structure was implemented in a 65 nm SOI process and extensive measurements were taken over multiple chips. The results showed about 100% leakage variation and 7% on-current variation over a 558 µm by 380 µm silicon area. The test structure serves as a prototype demonstration of a minimally invasive and low overhead approach that leverages the existing power delivery architecture and power control circuits such as power gating in actual product chips to obtain their variation characteristics.

REFERENCES

[1] Y. Lee *et al.*, "Temperature Rising Effect of 193nm Chemically Amplified Resist during Post-Exposure Bake", *SPIE*, vol. 3999, pp. 1000-1008, 2000.

[2] C. Berger *et al.*, "Critical Dimension Variations of I-line Processes due to Swing Effects", *SPIE*, vol. 6153, pp. 61523T, 2006.

[3] Y. Borodovsky, "Impact of Local Partial Coherence Variations on Exposure Tool Performance", *SPIE*, vol. 2440, pp. 750-770, 1995.

[4] A.K. Wong, R. Ferguson, S. Mansfield, "Mask Error Factor in Optical Lithography", *IEEE Trans. on Semi. Manuf.*, vol. 13, pp. 235–242, May 2000.

[5] D.G. Chesebro *et al.*, "Overview of Gate Linewidth Control in the Manufacture of CMOS Logic Chips", *IBM J. of Res. and Dev.*, vol. 39, pp. 189-200, Jul 1995.

[6] C. Hedlund, H. Blom, S. Berg, "Microloading Effect in Reactive Ion Etching", *J. of Vacuum Sci. and Tech.*, vol. 12, pp. 1962–1965, 1994.

[7] M. Bhushan, A. Gattiker, M. B. Ketchen, K. K. Das, 'Ring Oscillators for CMOS Process Tuning and Variability Control", *IEEE Trans. on Semi. Manuf.*, vol. 19, pp. 10–18, Feb. 2006.

[8] A. Gattiker, M. Bhushan, M. Ketchen, "Data Analysis Techniques for CMOS Technology Characterization and Product Impact Assessment", *Intl. Test Conf*, pp. 1-10, 2006.

[9] K. Agarwal, S. Nassif, "Characterizing Process Variation in Nanometer CMOS", *Design Automation Conf.*, pp. 396-399, 2007.

[10] K. Agarwal, D. Acharyya, J. Plusquellic, "Characterizing Within-Die Variation from Multiple Supply Port IDDQ Measurements", *International Conference on Computer-Aided Design*, pp. 418-424, 2009.