Power Supply Transient Signal Analysis for Defect-Oriented Test

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Abstract -- **Transient Signal Analysis (TSA) is a testing method that is based on the analysis of a set of V_{DD} transient waveforms measured simultaneously at each supply port. Defect detection is performed by applying linear regression analysis to the time or frequency domain representations of these signals. Chip-wide process variation effects introduce signal variations that are correlated across the individual power port measurements. In contrast, defects introduce uncorrelated local variations across these measurements that can be detected as anomalies in the cross-correlation profile derived (using regression analysis) from the power port measurements of defect-free chips. This work focuses on the application of TSA to the detection of delay faults.**

I. Introduction

A defect-oriented test method is based on a fault model that accurately abstracts some fraction (ideally all) of the analog circuit deviations introduced by defects to a set of discrete faults, that can be targeted by a set of tests and detected by production test and measurement equipment [1]. Such a method is particularly valuable if it can detect defects that no other method in the test suite can detect. Delay faults caused by resistive shorting and open defects are not well modeled by the traditional stuck fault model and are difficult to detect using structural test methods. In this paper, we propose a defect-oriented testing method called Transient Signal Analysis or TSA that may be capable of detecting these types of hard-to-detect defects.

In TSA, a set of power supply transients are measured simultaneously at the multiple power supply ports on the chip. A defect detection strategy that is based on the analysis of supply port signals offers several advantages. First, the connection between the measurement point (the supply port pad) and the source of the transient signals (the transistors) is unbuffered and low in resistance, and therefore the power ports pro-

vide a means of accurately measuring the temporal and frequency characteristics of the switching transients. Although the power grid resistance is small, the large size of the power grid and the current requirements of the core logic require the use of multiple, spatially distributed power port connections to the external power supply. This architecture creates multiple current paths between the transistors and the external power supply through the individual supply ports. However, the small differences in the resistance along these paths from any given point in the layout scales up the current in the supply ports that are topologically "close" to the switching transistors. This property of the supply grid provides the opportunity to distinguish between "local" disturbances, i.e. signal variations introduced by defects in nearby supply ports, and "global" process-induced variations, i.e. signal variations introduced in all supply ports caused by tolerable variations in process. In [2], we describe a procedure that exploits these properties and demonstrate its application to detecting functional failures.

Secondly, the supply transients reflect the delay characteristics of logic signal propagation in the CUT. In previous work, we describe an extension to the TSA method that is able to estimate path delays in defect-free CUTs through the analysis of the Fourier phase representation of the supply transients [3]. In this paper, we develop an analytical model for TSA and identify features that support the effectiveness of the phase representation for the detection of delay faults.

II. Background

Techniques based on the analysis of transient signals are described in [4-9]. The main drawback of these techniques is that they do not account for vector-to-vector or process variations. Therefore, they are difficult to apply to devices fabricated in advanced technologies, in which these types of variations are significant and must be accounted for.

The ECR I_{DDT} method accounts for process variation effects by computing ratios from the time domain I_{DDT} waveform areas measured under different test sequences [10]. The effectiveness of ECR was later demonstrated on lower power biomedical ICs in [11][12]. The results of research in [13] suggest that defect detection metrics based on RMS values of I_{DDT} are best accompanied by frequency metrics. Although the

experiments were performed on analogue devices, enhanced detection of resistive bridges and opens was possible when the I_{DDT} RMS value was used in combination with the first five Fourier Magnitude components. A method that additionally considers the effects of process parameter variations is proposed in [14].

The technique proposed in this work differs from previous work in several significant ways. First, the method explicitly accounts for process and vector-to-vector variation effects by cross-correlating the power supply transient signals measured at individual supply ports on the CUT. Second, in addition to the Fourier magnitude and RMS values of the supply transients, we have determined that the Fourier phase spectrums can be used for defect detection and may be the most effective representation for the detection of delay faults [15].

III. Path Delay, I_{DDT}, and Fourier Phase

As indicated above, the relationship between the functional and delay characteristics of the core logic and the supply transients (I_{DDT}) is cause-effect. A simple model is constructed by decomposing the I_{DDT} waveform into its constituent gate-generated I_{DS} waveforms. For example, the left side of Figure 1 shows a string of inverters and their corresponding I_{DDT} and I_{DS} waveforms. The right side gives SPICE simulation results showing the input waveforms driving gates G_m and G_n and the corresponding I_{DS} waveforms. Vertical lines are drawn through the 50% points in the input waveforms and through the peak tops in the I_{DS} waveforms. The two horizontal arrows are the same length, illustrating the correlation between delay and these features of the I_{DS} waveforms. The I_{DDT} generated on the supply grid is the superposition (via a linear RC network) of these individual I_{DS} transients. Therefore, variations in delay, e.g. due to process variations, scale the corresponding I_{DDT} waveform in time.

Although this analysis indicates that the width of the I_{DDT} waveform can be used to approximate delay, there are several other factors that may reduce the accuracy of this strategy in practice, including the RLC components of the power delivery system, the propagation of signals along multiple paths and the measurement noise introduced by the test environment [16]. Alone or in combination, these factors can distort the I_{DDT} signals measured at the power ports. A Fourier phase analysis of I_{DDT} may be more accurate under

these conditions since the analysis can be focused on frequency bands that are not significantly affected by these factors.

Phase is related to the I_{DDT} transients through a Fourier property given by Eq. 1. This property indicates

$$x(\alpha t) \overset{\mathcal{F}}{\Leftrightarrow} \frac{1}{|\alpha|} X\left(\frac{\omega}{\alpha}\right) \qquad \text{where } \mathcal{F} \text{ indicates the Fourier transform.} \qquad (1)$$

that scaling a time domain waveform by α scales the phase components by $1/\alpha$ in frequency. As an illustrative example, Figure 2 shows the power supply transient waveforms from simulations of a circuit (not shown) in which two paths are sensitized under three process models. The simulation runs are labeled P_1 (slowest process) through P_3 (fastest process). Here, V_{DDT} waveforms are shown instead of I_{DDT} waveforms. V_{DDT} is related to I_{DDT} through the linear RLC elements of the probe card model. The main advantage using V_{DDT} signals over I_{DDT} is that they can be measured "non-invasively" using high resolution voltage sampling instrumentation. This is an attractive feature in a production test environment, particularly given the usual space limitations in and around the test head and wafer handling system. (Reference [16] presents other details of the CUT and probe card model.)

In the following, the two paths are referred to as the $Path_A$ and the $Path_B$. The delays along these paths are not well correlated due to differences in the widths of the transistors defining the gates of the two paths. Therefore, it is not possible to accurately estimate the delays along both paths using the V_{DDT} transients generated on the unified supply rail. However, the larger transistors composing the gates along $Path_B$ in this circuit cause the I_{DS} contributions of the $Path_B$ gates to dominate those generated by the $Path_A$ gates. The more significant contribution of the $Path_B$ on the V_{DDT} has a corresponding larger influence on its Fourier phase components, and causes the lower frequency phase components to track the delay along the $Path_B$ more closely [15]. However, the higher frequency phase components are distorted by the contribution of the uncorrelated $Path_A$, as shown on the left of Figure 3. The ability to select a frequency band that excludes the distortions introduced by $Path_A$ improves the accuracy of estimating the $Path_B$ delay. This demonstrates one advantage of using the phase representation of V_{DDT} over the time domain representation. A second

advantage related to tester RLC distortion is identified in the numerical analysis give below.

In [16], we reported the differences in path delays along $Path_B$ under process models P_2 and P_3, with respect to P_1, as 186ps and 334ps, respectively. These are the delays that we would like to track using the V_{DDT} transients. However, as indicated in the figure, the estimation of delay, given by measuring the distance at the falling edge of the V_{DDT} transients as shown in the figure, yields 169ps and 424ps, respectively. In contrast, Figure 3 shows the phase spectrums of these signals through 1.5GHz. The frequency components between 300 and 900 MHz are nearly linear. As indicated above, the higher frequency components (> 900 MHz) are non-linear and distorted by the contribution of $Path_A$. The lower frequency components (< 300 MHz) are distorted by the RCL components in probe card. The delay estimation using the phase shifts in the 300-900 MHz range are 201ps and 324ps, respectively (see ref [16] for details on the procedure).

IV. TSA For Detecting Delay Faults

As indicated in the introduction, the low impedance, unbuffered property of the power grid and its ports makes it possible to accurately measure the frequency components of the switching transients. However, the non-zero resistance of the grid in combination with multiple ports and the presence of on-chip decoupling capacitance, "localize" the switching transients to supply ports that are topologically close. Therefore, spatial variations in the CUTs performance are captured in the set of supply port signals. Under a global process variation model, local performance variations are expected to be small across layout regions that span several supply ports. Any significant local change in performance can then be interpreted as a delay fault. In order to identify the local variation resulting from a delay fault, it is necessary to exercise multiple paths, some of which are defect free. The detection strategy can then correlate the individual supply port signals and look for differences or non-correlations in the performance estimates. Ideally, the analysis should be insensitive to the correlation in supply port signals that result from global performance variations.

These concepts are illustrated using the generic power grid for a peripheral pad frame shown in Figure 4. Six power supply pads are shown interleaved within the GND and I/O pads. The grid itself is layered verti-

cally and routed across all layers of metal. The RC profile of the grid suggests that the transients generated by transistors in the region labeled *m* (*n*) will be larger in the supply pad signals measured at V_{DD1} (V_{DD5}) than in the other supply ports. Under a global process variation model, the circuit parameter values are expected to be similar in these regions, allowing the signals measured at V_{DD1} and V_{DD5} to remain correlated. In contrast, a delay fault along a path in region *m* will change the performance and corresponding signals in the V_{DD1} supply port. The lack of correlation in the V_{DD1} and V_{DD5} supply port signals can be detected by comparing the expected behavior of these supply port signals (obtained from other defect-free chips) with the measured performance.

One difficulty in performing an analysis that correlates the V_{DDT}s measured at multiple power ports is dealing with multi-data point waveform representation. In order to provide a practical solution, a more efficient representation of the waveforms is needed. Also, tester environment noise, e.g. EMI, was identified, but not treated, as a factor that reduces the accuracy of the analysis in the previous section. The most straightforward means of removing systematic noise sources is to compute waveform differences. This can be accomplished in the time or frequency domain by subtracting, point-wise, the CUT's V_{DDT} time or phase waveforms from a corresponding set of "golden" device waveforms. The simplest way of generating the "golden" device waveforms is to apply tests to a known defect-free chip. The difference operation removes the noise introduced by the tester electronics, and produces a difference waveform called a Signature Waveform or SW that represents only the chip-to-chip variation. One way of compacting the signal information in the SWs is to compute the areas under their curves. In previous works, we show that the Signature Waveform Areas (SWAs) work well in a "cross-correlation" detection procedure based on linear regression analysis [2], and demonstrate a hardware circuit capable of computing them in [17].

As an illustrative example of the TSA process, Figure 5 shows two columns of phase SWs obtained from supply pads V_{DDx} and V_{DDy} from eight simulations of a test chip (see reference [2]). The same input sequence was used in the 8 simulations. The first simulation was performed on the defect-free nominal device and its results were used to generate the seven pairs of phase SWs shown in the figure. The pairs of

SWs in the top 6 rows correspond to simulations on circuit models in which the transistor mobilities (μ_0) were varied globally by the amounts shown in the figure. The SWs from these simulations capture the signal variations produced under these simple process models (PM). The last row shows the SWs from a bridging experiment, B-PM_D, in which the defect produces a delay fault. Process model *D* was used in this "faulted" simulation.

In Figure 5, the 12-24 MHz frequency band is delimited by vertical lines. It is within this region that the SW pairs in the first 6 rows are most strongly correlated. In [3], we further demonstrate that the areas under both the V_{DDx} and V_{DDy} SWs in this region correlate closely to the measured performance of the chips under these process models. In order to identify the delay defective chip, the correlation profile defined by area pairs under the first six defect-free devices is used to establish the defect-free process space as shown in Figure 6. Here, the areas (SWAs) computed over the 12-24 MHz band for each SW pair are plotted along the x and y axis, respectively, in a scatter plot. The data points for PM_A through PM_F track linearly, as shown by the regression line. The process space, called the process variation zone or PVZ, is delimited by 3σ prediction limits. The PVZ accounts for variations in the SWA ratios caused by intra-device process variations, e.g., changes in the RC-transistor parameters of a single conductor or transistor type over a region of the chip, the lack of correlation in the variations of the RC-transistor parameters of different conductors or transistors, and measurement noise.

In contrast, the ratio of the SWs labeled *Def* along the bottom-right of Figure 6 is not closely approximated by the same ratio that characterizes the SWs from process model simulations. The defect introduces significant regional variation in the SW of V_{DDx} due to its proximity to this supply port. In contrast, the RC components of the supply grid attenuate the variation introduced by the defect at the more distant V_{DDy} supply port, whose signals more closely track the local performance of the defect-free paths in that region. Since process model *D* was used in the bridging experiment, the local variation in V_{DDy} is expected to be similar in magnitude to the defect-free process simulation result. This is evident in the V_{DDy} B-PM_D and PM_D phase SWs in Figure 5. The large local variation in V_{DDx} in combination of the smaller variation in

V_{DDy} under the B-PM_D simulation produces an outlier data point in Figure 6, allowing this chip to be identified as defective.

V. Conclusions

A simple analytical model is derived that relates propagation delay with features of the power supply transients. The extension of the model to the frequency domain demonstrates that the phase representation of the supply transients can be used to track delay. The RC attenuation characteristics of the supply grid in combination with the multiple supply ports allows local performance variations to be identified. Under a global process model, local changes in the performance can be attributed to the presence of a delay-oriented defect. Linear regression analysis can be used to identify anomalies across the supply port measurements of a chip that result from delay faults.

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Figure Captions

Figure 1. Inverter chain (left), SPICE input waveforms driving inverters *m* and *n* and I_{DS} (left).

Figure 2. V_{DDT} waveforms from Process simulations.

Figure 3. Unwrapped Phase spectrums of V_{DDT} waveforms shown in Figure 2.

Figure 4. Generic power grid in a peripheral pad frame.

Figure 5. Vdd_x and Vdd_y phase Signature Waveforms from 8 simulation experiments.

Figure 6. Scatter plot, regression line and prediction limits (process variation zone or PVZ) using data from Figure 5.

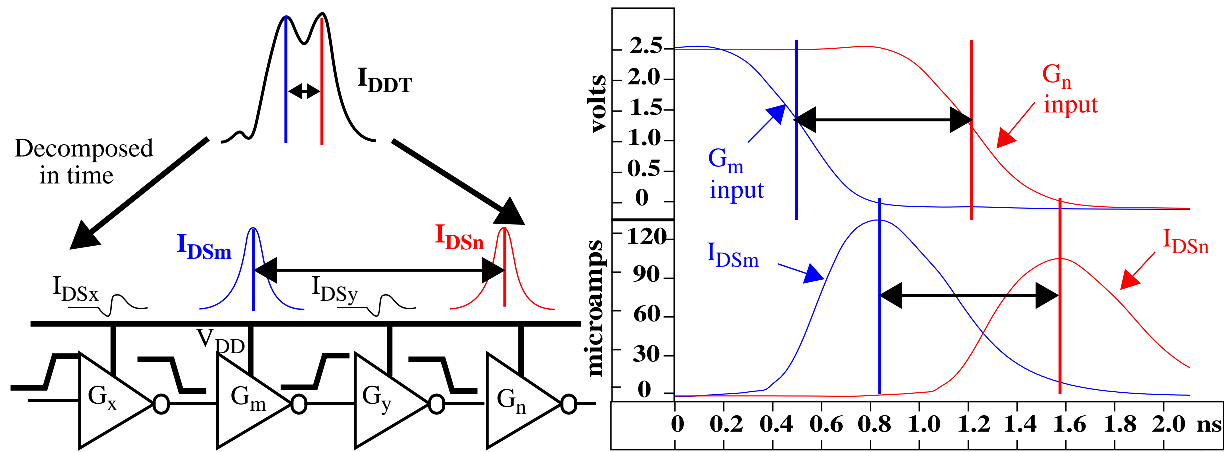

Figure 1

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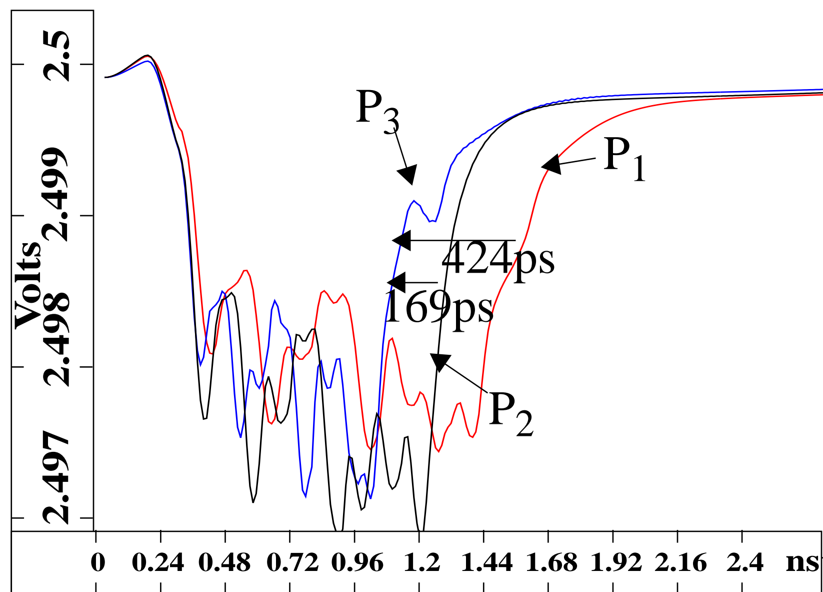

Figure 2

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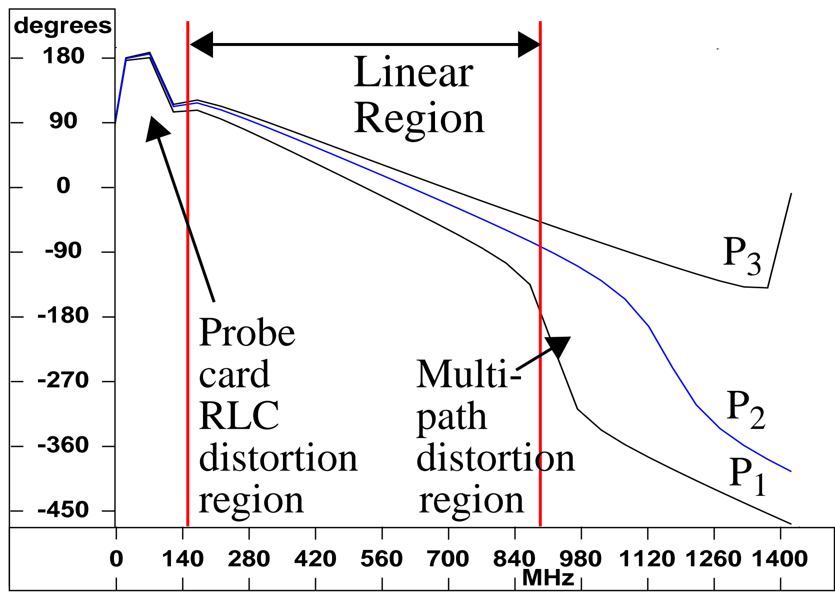

Figure 3

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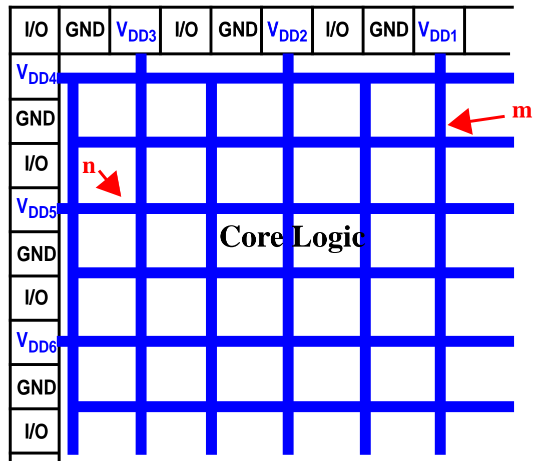

Figure 4

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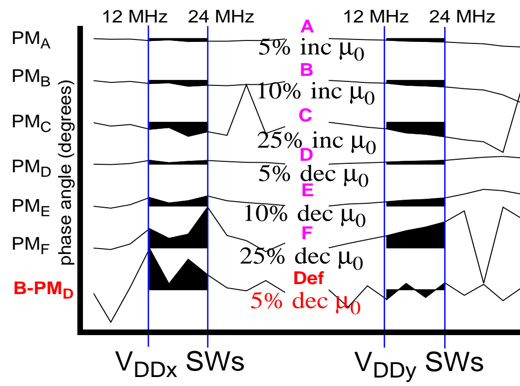

Figure 5

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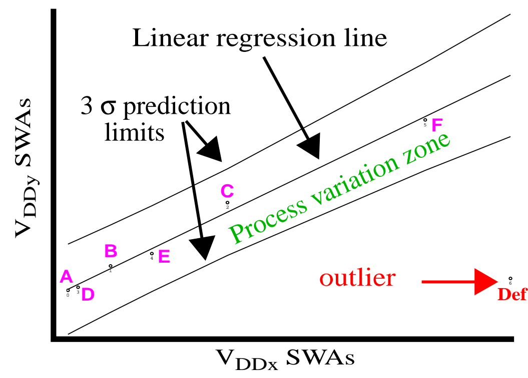

Figure 6

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