Measuring Power Distribution System Resistance Variations

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Abstract -- **Metal resistance variations in back-end-of-line processes can be significant, particularly during process bring-up. In this paper, we propose a simple method to measure resistance variations in the power distribution system (PDS) of an IC. Our technique utilizes the PDS because it is an existing distributed resource in all ICs and provides a means of characterizing resistance in the context of the actual circuit design. By applying a set of tests using small on-chip support circuits attached to the PDS, the resistance of components of the PDS can be obtained from the solution to a set of simultaneous equations. The results from hardware experiments involving two sets of test chips fabricated in an IBM 65 nm technology show significant changes in the resistance variation of some components of the PDS as the process evolved.**

Index terms -- **process variation, power distribution system, resistance variations**

I. Introduction

It is widely accepted that the level of systematic and random process-induced variations in devices and interconnect is increasing as technologies are aggressively scaled [1][2]. The sources of lithographic and non-lithographic process variations continues to grow [3-7]. Process variations impact key electrical parameters, including Vt, resistance and capacitance, and have a significant impact on power and delay. For advanced technologies, it becomes increasingly important to track process variations to avoid delays in time-to-market. In particular, new methods and test structures are needed to reduce manufacturing development and yield learning cycle times and to support rapid product and process debug.

The focus of this work is on the design and implementation of a test infrastructure that supports the measurement of power distribution system (PDS) resistance characteristics for tracking back-end-of-line (BEOL) process variations. The method is designed to enable a fast, first order analysis of metal resistivity,

and to facilitate the identification of process problems. It also serves to enable the resistance characteristics of the PDS to be evaluated for validation purposes, and provides meaningful data in the context of an actual circuit design, as opposed to the use of test structures.

Our specific goals are to estimate the off-chip resistance components of the PDS and several on-chip components of the power grid using voltage and current measurements. An important design criteria is to enable the measurement of resistance on any portion of the PDS stand-alone, i.e., without the need to measure the resistance components of the entire PDS, and to do so using as little on-chip support circuitry and off-chip instrumentation as possible.

In this paper, we propose a test infrastructure that meets these goals, along with a set of equations that can be solved simultaneously to yield various resistance components of the PDS. The method is applied to two sets of chips, one set fabricated during early phases of process bring-up and a second set fabricated after process improvements were made. Standard statistical methods are used to characterize the resistance variations in the PDS of the chips. The results indicate that the magnitude of the resistance variations in the lower levels of the PDS are significantly smaller in the second set of chips.

The remainder of this paper is organized as follows. Section II provides an overview of existing, related work on process variation measurement techniques. Section III describes features of our test chip and the equivalent resistance models that we derived for the PDS, as well as the procedure and tests necessary to determine the resistance of various PDS components. Section IV presents the experimental results and Section V gives our conclusions.

II. Background

There is a wide spectrum of published work on measuring and analyzing process variations. References [8-18] provide a sample of recent work. The techniques proposed in references [8] through [13] make use of ring oscillators and other types of test structures to track variations in front-end-of-line parameters (FEOL) or single wire/via in BEOL parameters. For example, in [8], the authors propose a logic characterization vehicle to investigate the yield and performance impact of process variations. Digitally configurable

ring oscillators are proposed in [9] to measure of the effects of process variations on performance. A framework is presented in [10] for the statistical design of experiments to measure the variance in critical dimension of gate poly-silicon. A test structure is proposed in [11] to measure cell-to-cell delay mismatch due to process variations, and in [12], for the statistical characterization of local device mismatches. The authors of [13] propose a test structure that enables the extraction of spatial and layout dependent variations in both transistor and interconnect structures.

Techniques proposed in references [14-18] focus on the measurement and analysis of resistance variations, but again, the work is limited to single wire and/or vias. For example, [14] and [15] proposes test structures for characterizing wire resistance mismatch. Resistance measurement and analysis techniques for linewidth and step variation are described in [16] and [17]. Reference [18] describes dishing and erosion in non-ideal copper CMP and proposes dummy feature insertion techniques to reduce its impact on resistance variations. To our knowledge, this is the first time a technique has been proposed for measuring resistance variations in the PDS.

III. Test Chip Characteristics, Power Grid Model and Resistance Measurement Procedure

This section of the paper is organized into several subsections. We describe the architecture of the power grid, the on-chip support circuitry and the experiment setup in Section III.A. We develop a power grid equivalent circuit model in Section III.B, and validate it with experimental data. The experimental procedure for carrying out PDS resistance measurement tests is given in Section III.C. The simultaneous equations that need to be solved to obtain the resistance components of the PDS are described in Section III.D. The resolution limits of our experiment are discussed in Section III.E.

The results reported in this paper are derived from chips fabricated in a 65 nm technology, and therefore are meaningful to state-of-the-art practices. However, the PDS measured in the hardware experiments was not designed to minimize *IR* and *L di/dt* voltage drops, and from this perspective does not conform to a typical PDS of a commercial product. In particular, the resistances of many of the PDS components of our test chips are larger, some by more than an order of magnitude, over those found in commercial chips. In order

to validate our technique for commercial applications, we supplement our test chip results with data from a simulation model that is representative of commercial designs.

A. *PDS Architecture*

A high-level representation of the power grid architecture used in the simulation and hardware experiments is shown in Figure 1. The bottom portion shows that adjacent metal layers are routed at right angles to each other in a mesh configuration with vias placed at the intersections. The GND grid (not shown) is interleaved with the power grid and routed in a similar fashion. Both grids are routed across the ten metal layers available in the 65 nm process. The width of the wires and the granularity of the mesh vary across the metal layers. In particular, the widths of the lower metal wires are smaller and the granularity is finer than the widths and granularity of the metal wires in the upper layers. This feature of the power grid is typical of commercial designs [19].

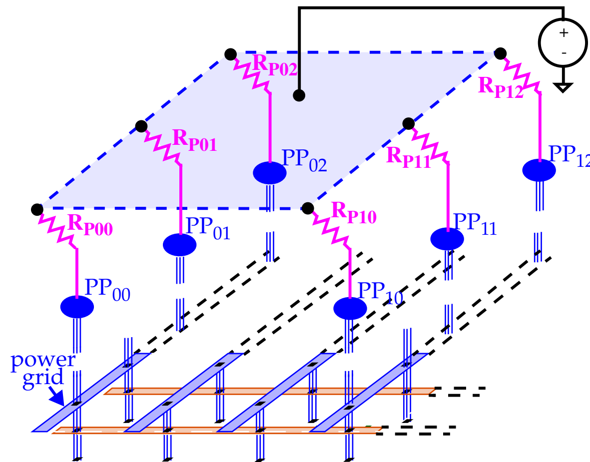

Figure 1. Power Grid Architecture

The power grid is connected to a set of six C4s or **power ports** (**PPs**) in the top metal layer. The PPs are shown as ovals in the figure and are labeled PP_{00} through PP_{12}. Commercial power grids can have 100s of such PPs. The C4s enable the power grid to be connected to the power supply, either through a membrane style probe card (during wafer probe) or through the package wiring. The finite resistance of PP connections are represented as series resistances, Rp_{xy}, in the figure.

The measurement technique proposed in this work requires the measurement of branch currents through

each of the PPs. For packaged chips, the PPs are typically wired into a power plane(s) within the package before being routed off chip through the power pins. Therefore, it is not possible to apply our technique directly to packaged parts without additional on-chip support circuits (beyond those described herein). We assume in the remainder of the paper that our technique is applied at wafer probe, where it is possible to access the PPs directly.

In our test setup, we emulate a wafer probe environment in our packaged chips by dedicating a separate pin for each of the six PPs. The details of the test jig are shown in Figure 2. The package pins that are connected to the PPs wire onto a PCB to a set of six mechanical, low resistance switches. The switches can be configured in a left or right position. The left and right outputs of the switches each connect to a common wire that is routed to the *global current source meter* (GCSM) and *local current ammeter* (LCA), respectively, as shown in the figure.

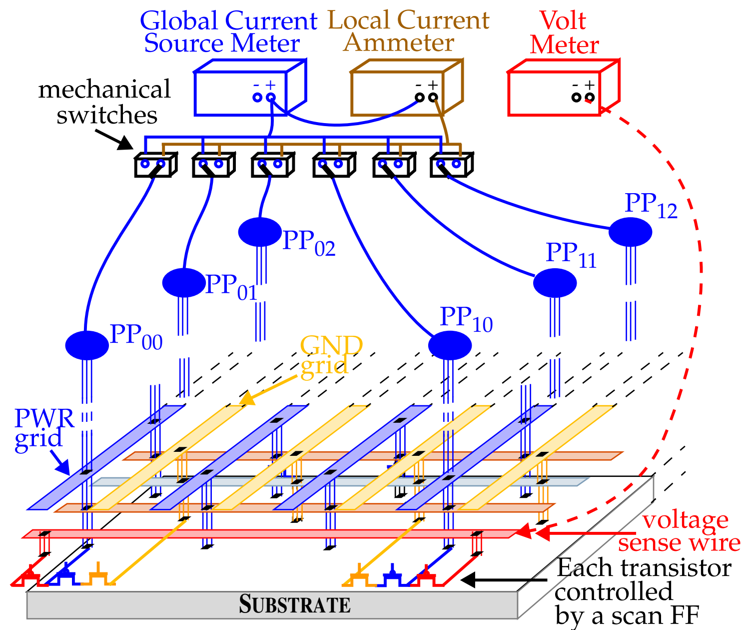

Figure 2. Instrumentation Setup

The GCSM provides 0.9 V to the PDS and can measure current at a precision of approximately 300 nA. The LCA is wired in series between the switches and the GCSM and allows measurement of the individual PP (*local*) currents at the same level of precision. For example, the switch configuration in Figure 2 allows measurement of the local PP$_{00}$ current, I_{00}, as well as the global current.

In addition to the branch currents, our technique to measure resistance also requires on-chip voltage measurements. The voltage is measured in our experiments using a seventh pin, that is connected internally to a globally routed voltage sense wire (VSW). A voltmeter is connected to this pin off-chip, as shown in Figure 2.

The last element of the test infrastructure is shown along the bottom of Figure 2 and in more detail in Figure 3. A resistance measurement circuit (RMC) is inserted under each of the six C4s. The RMC consists of *stimulus transistors*, a *voltage sense transistor* and a set of three *scan flip-flops* (SFFs). The outputs of the SFFs connect to the gates of the three transistors as shown in Figure 3(b)[1]. The stimulus transistors provides a controlled stimulus, i.e., a short between the power and ground grid, when the states of the SFF_1 and SFF_2 are set to 0. The voltage on the metal 1 layer of the power grid is measured using the voltage sense transistor, enabled when a 0 is placed in SFF_3.

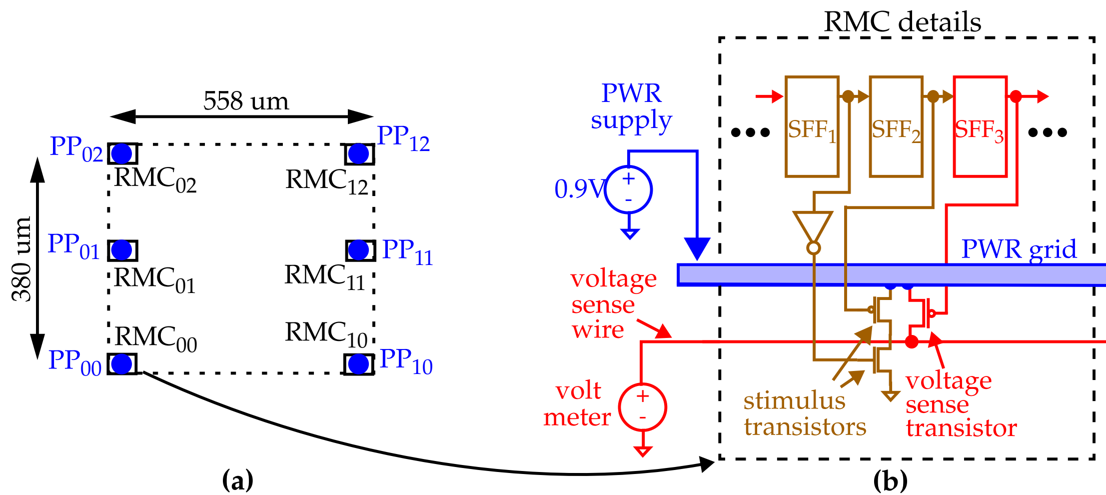

Figure 3. (a) Block diagram of the test structure and (b) details of the resistance measurement circuit (RMC).

B. Power Grid Equivalent Circuit Model

The equivalent resistance models shown for the power grid in Figures 4(a), 4(b) and 4(c) were deduced from SPICE DC simulation data collected from a resistance model of the test chip's power grid. The power

[1] The stimulus as shown in our test structures was designed to serve other purposes beyond those described in this paper. A more efficient implementation would use only the p-channel transistor portion of the series transistor pair.

grid resistances, given as R_x, R_y and R_z, represent the equivalent resistance of an entire mesh of resistors in the simulation model. The resistances R_{p1} and R_{p2} represent the external connection or *probe* resistances to the power grid.

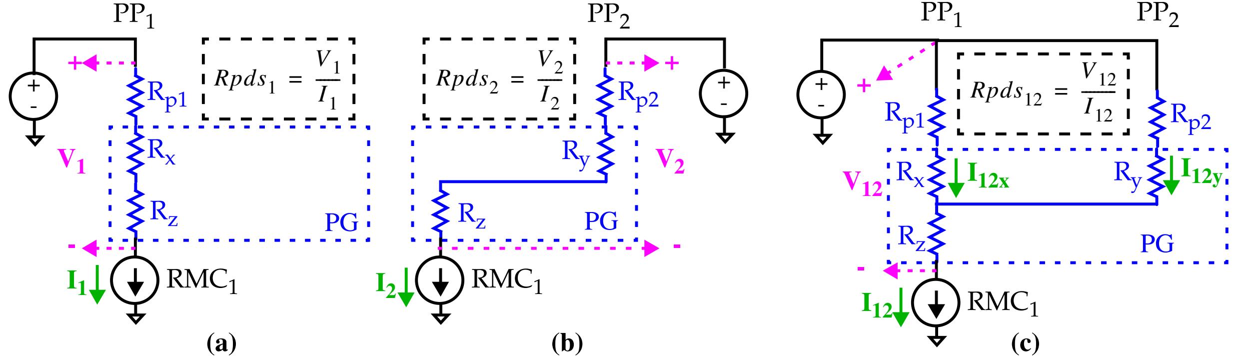

Figure 4. 1-port and 2-port power-up schemes to determine appropriate resistance model.

The models shown in Figures 4(a) and 4(b) are referred to as 1-port experiments because only one PP is connected to the power supply. The configuration in 4(c) is called a 2-port experiment. The stimulus in each configuration is provided by RMC_1, which is depicted as a current source. The currents and voltage drops are labeled symbolically for each of the three experiments, e.g. I_1 and V_1.

Our objective is to verify that the equivalent resistance models of Figure 4 are valid representations of the actual PDS. Assuming this is true, then Equation 1 expresses the relationship between the equivalent resistances in the three models, i.e. $Rpds_1$, $Rpds_2$ and $Rpds_{12}$. Each of these is defined as V_x/I_x where V_x is the voltage drop and I_x is the total current, for $x = 1, 2$ or 12 (see dashed boxes in figure). For example, the first

$$Rpds_{12} = \frac{1}{\underbrace{\frac{1}{(Rpds_1 - R_z)}}_{R_{p1}+R_x} + \underbrace{\frac{1}{(Rpds_2 - R_z)}}_{R_{p2}+R_y}} + R_z \quad (1)$$

element on the right side of the equation gives the parallel resistance of the upper network in Figure 4(c) expressed using the equivalent resistances in Figures 4(a) and 4(b). The second element on the right side of the equation accounts for the shared resistance, R_z, that is in series with the parallel network.

We confirmed these models using a numerical analysis of data collected from a simulation model and

from one of the 65 nm test chips. The values of the equivalent resistances that we computed are presented in Table 1. Columns two, three and four give the equivalent resistances computed using data from the configurations shown in Figures 4(a), 4(b) and 4(c), respectively. The measured value of $Rpds_{12}$ agrees with the value predicted by Equation 1. The R_z values in column five are derived by solving Equation 1 for R_z.

	$Rpds_1$	$Rpds_2$	$Rpds_{12}$	R_z	R_x	$R_z/(R_x + R_z)$
Simulation Data	14.05 Ω	20.04 Ω	12.10 Ω	8.18 Ω	0.63 Ω	92.9%
Hardware Data	14.24 Ω	20.02 Ω	12.27 Ω	8.38 Ω	0.62 Ω	93.1%

Table 1: Numerical analysis of 1-port and 2-port simulation and hardware experiments.

The series resistance combinations $R_{p1} + R_x$ and $R_{p2} + R_y$ are represented by the terms in the denominator of Equation 1 as indicated above. However, the three tests as shown in Figure 4 are not sufficient to determine the individual values, e.g. R_{p1} and R_x. We were able to derive the individual values by creating a simulation model that closely approximates one of our test chips[2]. The estimated values for R_{p1} and R_{p2} derived in this fashion are 5.24 Ω and 11.71 Ω, respectively.

The values of R_x and R_y are easily obtained once R_{p1} and R_{p2} are known. The R_x values are given in column six of Table 1 (the R_y values are similar). When compared with the R_z values in column five, it is clear that R_x is smaller by more than an order of magnitude. Given that R_x and R_z are both grid equivalent resistances, this data illustrates that the paths followed by the branch currents I_{12x} and I_{12y} from Figure 4(c) are common over a large fraction of the vertical resistance of the PG. Column seven of Table 1 gives the fraction at nearly 93%. The wire characteristics described for the PG in Section III.A support this finding. There, we disclosed that the resistance of the wires in the upper layers of the PG is smaller than the resistance of the wires in the lower layers.

Our simulation model enabled a more detailed investigation of the spatial distribution of currents through the PG. Figure 5 shows a 3-D voltage profile for the 2-port simulation model with RMC_{00} enabled (see Figure 3(a)). The voltage potential surfaces of both the top-most metal layer and bottom-most metal layer are

[2]. The actual values can be measured by adding voltage observe points in the PG's top metal layer directly beneath the C4s.

superimposed. For most of the *x-y* dimension of the grid, the top and bottom surface potentials are nearly identical, indicating that current from remote PPs, e.g. PP_{01}, remains in the top portion of the grid until reaching the potential well near PP_{00}. At this point, the branch currents from different PPs combine and traverse the majority of the vertical dimension together. This type of current behavior will tend to amplify the magnitude of local IR drops.

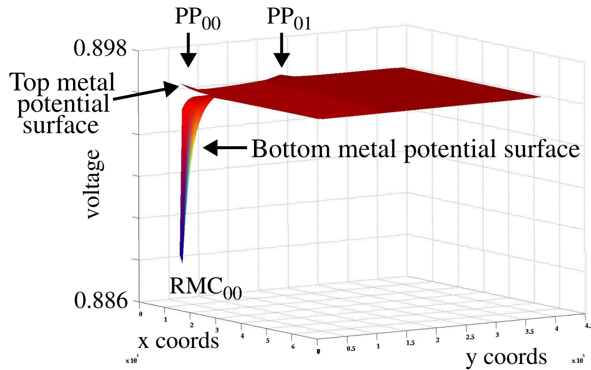

Figure 5. Top and bottom voltage profile of 2-port simulation experiment of the test chip grid.

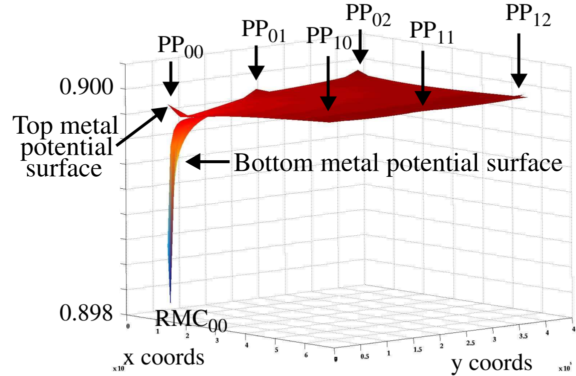

Figure 6. Top and bottom voltage profile of 6-port simulation experiment of a commercial grid.

We re-extracted our power grid with much smaller via and resistance-per-square resistivities to determine how the values in Table 1 would change for a PDS that better represents a commercial design. The Rps were also reduced by a factor of twenty to model the contact resistance of a typical probe card. The voltage profile of this grid is shown in Figure 6 and its resistance characteristics are given in Table 2. $Rpds_{00}$ is the equivalent resistance measured with RMC_{00} enabled. It is a factor of eight times smaller than the value in column two of Table 1. The lower resistances of the metal wires in this model are also reflected in columns three and four. However, the fraction in column five is still significant at 80.6%, and therefore, the lower resistivity of this grid only partially explains the current distribution characteristics. We determined using other grid configurations that the most significant factor affecting this fraction is the architecture of the PG. For example, PGs configured such that each layer has the same resistance produce a fraction of 50%.

	$Rpds_{00}$	R_z	R_x	$R_z/(R_z + R_x)$
Simulation Data	1.74 Ω	1.47 Ω	0.35 Ω	80.6%

Table 2: Numerical Analysis of 6-port experiments of low resistance PDS.

C. PDS Resistance Measurement Tests

Our goal is to define a set of tests that provide data to solve for six unknown resistances in the PDS. The three tests and corresponding equivalent circuit models are shown in Figures 7, 8 and 9. The six resistances, two of which are the sum of two series resistances, are labeled as $Rpv_a = Rp_a + x$, Rv_a, $Rpv_b = Rp_b + y$, Rv_b, Rh_a and Rh_b, where 'p' indicates *probe*, 'v' denotes *vertical* and 'h' denotes *horizontal*. As noted in the previous section, is not possible to separate the series resistances, e.g. $Rp_a + x$, unless capability is added to the infrastructure to allow the voltage to be sensed at the point where the C4 attaches to the power grid.

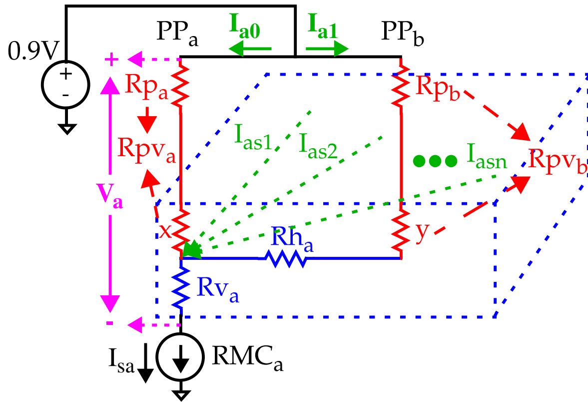

Figure 7. Complete model: 1st test.

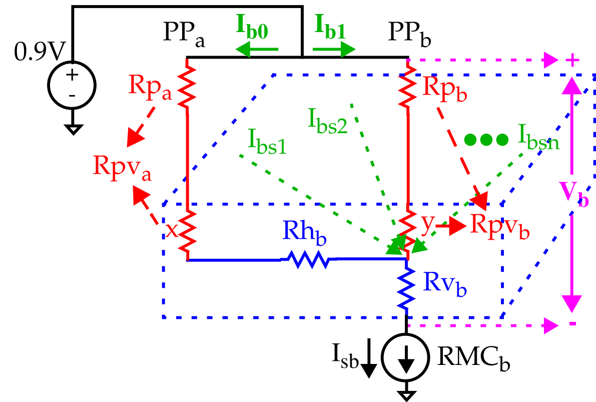

Figure 8. Complete model: 2nd test.

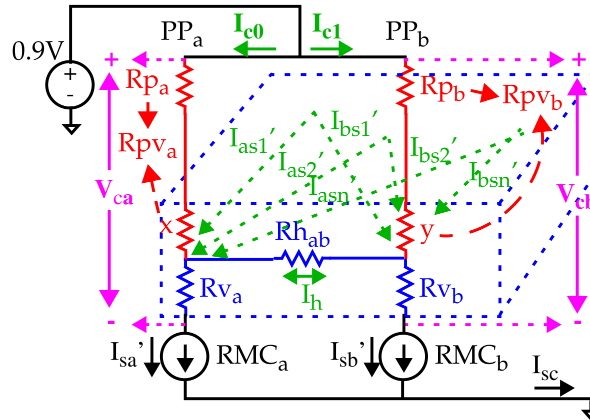

Figure 9. Complete model: 3rd test.

According to the models, Rh_a, Rh_b and Rh_{ab} identify the same resistance and therefore, represent only a single unknown. From simulation experiments, we find there are actually small differences in these resistances. The equations that we present later treat Rh_a and Rh_b in a special way and as separate variables. The

values derived from our equations represent a good estimate of Rh_a, Rh_b and Rh_{ab}.

Each test provides two independent equations, enabling values to be derived for the six resistances from the solution to a system of simultaneous equations (to be described). The third test shown in Figure 9 requires enabling both RMC_a and RMC_b and measuring two voltages, V_{ca} and V_{cb}. Under the proposed infrastructure, it is necessary to measure each of these sequentially by enabling the appropriate voltage sense transistor.

The current and voltages shown in Figures 7, 8 and 9 are calibrated to remove the impact of leakage currents. This is an important step to obtaining a meaningful result in modern technologies, given the trend of increasing background leakage currents. Calibration is carried out by measuring the currents and voltages, as given in Figures 7 and 8, under a forth configuration in which both RMC_a and RMC_b are disabled. These values are subtracted from the values measured under the three tests.

Branch Current Calculation

Unlike the 1-port and 2-port experiments shown earlier, the multi-port scheme introduces a set of additional currents, such as those labeled I_{as1}, I_{as2} through I_{asn} in Figure 7. These currents originate from the PPs distributed across the PG. The total current, e.g. I_{sa} in Figure 7, includes their contribution. Although it is straightforward to compute these supplementary currents, only the total current is needed in the equations given in the next section[3].

The only currents that cannot be measured individually are the stimulus currents, I_{sa}' and I_{sb}', shown in Figure 9. They are labeled using the *prime* symbol because they are related to the 'unprimed' values measured under the first and second tests. Under ideal conditions, the current sum, $I_{sa} + I_{sb}$, measured under the first and second test, is equivalent to $I_{sa}' + I_{sb}'$ (or I_{sc}). However, the p-channel stimulus transistors are not ideal current sources, and the small change in V_{DS} introduced by having both RMC_a and RMC_b enabled reduces their magnitudes.

In our experiments, the difference is small, i.e. at most a couple uAs, and can be derived using Equation

[3]. In our experiments, we compute the total current as the sum of the calibrated power port currents.

2. The currents on the right side of the equation are the total currents measured under each of the three tests.

$$\Delta I_s = I_{sa} + I_{sb} - I_{sc} \quad (2)$$

From simulation experiments, we determined that the reduction in current given by ΔI_s splits nearly equally across both RMC_a and RMC_b in the third test. This holds under the condition that the resistance characteristics of the PDS as measured from either stimulus location are similar -- a reasonable assumption given the uniform architecture of the power grid. We examined a variety of resistance configurations and found that the magnitudes of I_{sa}' and I_{sb}' are well approximated using Equation 3. The supplementary currents, e.g.

$$I_{sa}' = I_{sa} - \frac{\Delta I_s}{2} \qquad I_{sb}' = I_{sb} - \frac{\Delta I_s}{2} \quad (3)$$

I_{as1}', as well as the current across Rh_{ab}, e.g. I_h, as given in Figure 9, can also be derived but are not needed to solve the set of equations given in the next section.

D. PDS Resistance Equations

The first four equations are derived from the models shown in Figures 7, 8 and 9 using Kirchhoff's voltage law. Equations 4 through 7 yield values for Rpv_a, Rv_a, Rpv_b and Rv_b directly if solved as a set of simultaneous equations.

$$V_a = I_{a0} \bullet Rpv_a + I_{sa} \bullet Rv_a \quad (4)$$

$$V_{ca} = I_{c0} \bullet Rpv_a + I_{sa}' \bullet Rv_a \quad (5)$$

$$V_b = I_{b1} \bullet Rpv_b + I_{sb} \bullet Rv_b \quad (6)$$

$$V_{cb} = I_{c1} \bullet Rpv_b + I_{sb}' \bullet Rv_b \quad (7)$$

R_h Analysis

The equations that we use to compute values for Rh_a and Rh_b, Equations 8 and 9, are not consistent with Kirchhoff's voltage law applied to the models in Figures 7 and 8. In particular, Rh_a is multiplied by the total

$$V_a = I_{a1} \bullet Rpv_b + I_{sa}(Rh_a + Rv_a) \quad (8)$$

$$V_b = I_{b0} \bullet Rpv_a + I_{sb}(Rh_b + Rv_b) \quad (9)$$

$$Rh = Rh_a + Rh_b \quad (10)$$

current, I_{sa}, in contrast to the model, which indicates the multiplier should be the branch current, I_{a1}. Given that I_{a1} is strictly less than I_{sa}, the values obtained for Rh_a and Rh_b using Equations 8 and 9 underestimate the actual values. Interestingly, the sum of Rh_a and Rh_b using these equations produces a good estimate of their actual value, under the assumption that Rh_a is nearly equal to Rh_b as we noted above is reasonable. We use Rh to represent the sum as given by Equation 10.

To demonstrate that these equations provide a better estimate of the Rh resistances over those derived using Kirchhoff's voltage law (via Equations 11 and 12), we conducted a sequence of experiments using a variety of PP configurations. The criteria that we use to determine the best analytical form is based on the

$$V_a = I_{a1}(Rpv_b + Rh_a) + I_{sa} \bullet Rv_a \tag{11}$$

$$V_b = I_{b0}(Rpv_a + Rh_b) + I_{sb} \bullet Rv_b \tag{12}$$

consistency of the results across the different PP configurations. Intuitively, the values computed for the six resistances should remain consistent independent of the power-up scheme. This is not the case for Rh_a and Rh_b, however, if Equations 11 and 12 are used.

To show this, we computed the values of the six resistances using hardware data from each of the PP configurations shown in Figure 10. The upper portion of the figure shows four 2-port experiments while the bottom portion shows a 4-port and a 6-port experiment. For each of the four 2-port experiments, the three tests described in Section III.C were applied using a pair of RMCs located underneath the labeled PPs. These twelve tests were also applied to the 4-port and 6-port configurations.

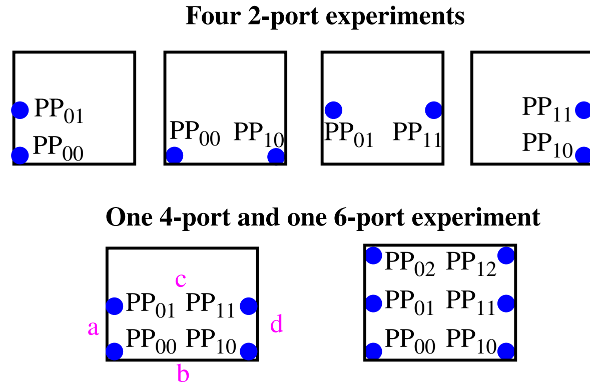

Figure 10. Power schemes investigated.

We first applied Equations 4 through 7 to derive values for each pair of Rpv's and Rv's under each of these configurations. For example, the resistances computed under the left-most 2-port configuration are Rpv_{00}, Rpv_{01}, Rv_{00} and Rv_{01}, labeled according to the PP coordinate space shown in Figure 10. The overlap of the PPs across the 2-port configurations allowed each of the four distinct Rpv's and Rv's to be computed twice, yielding a total of eight values. The same held true for the 4-port and 6-port experiments. The results are shown in Figure 11 as a set of curves. The two values computed for each variable are adjacent in the curves to illustrate that they are similar, as expected. The three curves for the 2-port, 4-port and 6-port experiments are superimposed to illustrate that there exists strong agreement among the computed values, independent of the PP configuration scheme. We conclude that Equations 4 through 7 give the appropriate analytical form for these resistances.

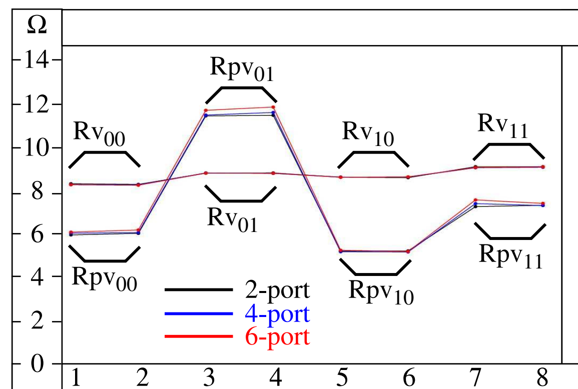

Figure 11. Rpv and Rv results under different power-up configurations.

We then carried out this analysis on Rh_a and Rh_b using Equations 11 and 12. The results are shown in Figure 12, but in a different format. The Rh_a and Rh_b values computed under each port configuration are offset in the x dimension (not superimposed as in Figure 11), and are labeled 2-port, 4-port and 6-port. The curves on the far right, labeled 'average Rh', are simply the average of the two curves for each port configuration on the left. The individual pairs of data points are labeled with the letters 'a' through 'd', to associate them with the positions given in the 4-port graphic shown in Figure 10.

The differences in the curves illustrate that Equations 11 and 12 are **not** of the appropriate form, particularly for the 4-port and 6-port configurations. We suspect that the supplementary currents, e.g. I_{as1} in Fig-

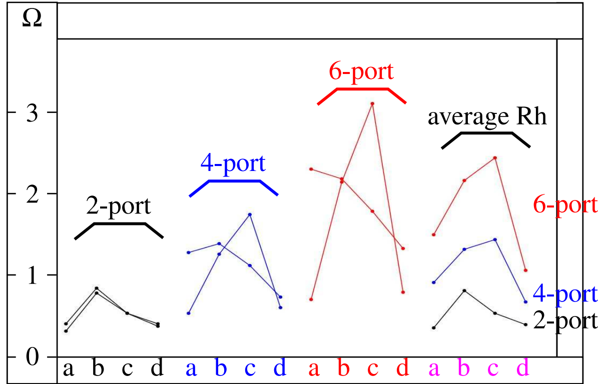

Figure 12. Rh values from Equations 11 and 12, with average Rh on right.

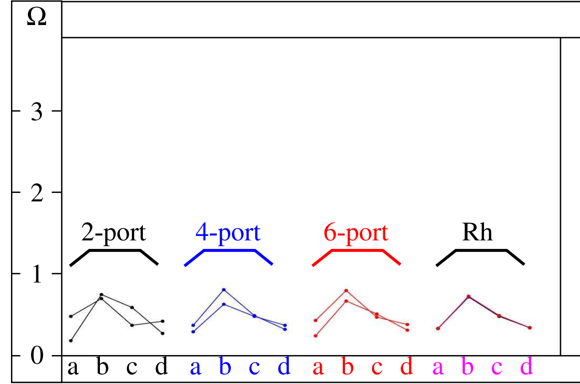

Figure 13. Scaled Rh values from Equations 8 and 9 (by 2x), with Rh sums using Equation 10 on right.

ures 7 and 8, are not properly represented by Equations 11 and 12. This is supported by the results obtained from the 2-port model, where the supplementary currents are zero. Here, the computed values for Rh are, in fact, good approximations of the actual values.

In contrast, the Rh values computed using Equations 8 and 9 across the various PP models are very similar, as shown in Figure 13. The curves are arranged in an analogous fashion to those in Figure 12, except in this case, the computed values are scaled up by a factor of two, to better illustrate their variation around the 'average' Rh values displayed in the curves on the far right. The similarity of the 4-port and 6-port curves with the 2-port curves suggests Equations 8 and 9 are better able to represent the resistance characteristics of the PDS. A major portion of the difference that remains in these curves is due to measurement noise, as described in the next section.

E. Noise Analysis

The large differences in the magnitudes of the resistances of the various PDS components and supporting infrastructure make it imperative to evaluate the resolution limits of the method. For example, the RMCs use transistors as the stimulus with DC resistances up to approximately 1000 Ωs. The resistances in the PDS of our chips vary over two orders of magnitude from a couple hundred mΩs to approximately 10 Ωs.

The limits are defined by the level of precision available in the instrumentation as well as the noise floor. We used Keithley 2400 precision source meters to collect the data. In our experiments, the noise floor is

approximately 300 nA when the Keithley is configured as an ammeter, and approximately 500 nV when configured as a voltmeter. The range of currents varied from a couple hundred uAs to a couple mAs, yielding approximately 5 digits of precision in the measurements. With the power supply voltage range set to 1.0 V, it was possible to get approximately 6.5 digits of voltage precision from the instrumentation. Given these measurement limits and resistance characteristics, resistance resolution is estimated to be approximately 100 mΩs.

This approach to calculating resistance resolution, however, ignores other detractors such as temperature effects, i.e. the temperature variation that occurs while the data is collected. The most straightforward way of accounting for all sources of error is to repeat the data collection process on the same chip multiple times and then to use statistics to characterize the resistance variations. We collected twelve sets of data from one of the chips, and then computed mean and standard deviation statistics on the resistance values derived from the equations.

The experiments were performed with all six PPs connected to the power supply as shown in Figure 14. The set of experiments consisted of applying the three-test methodology described in Section III.C to eleven pairings of the supply ports. Seven of the pairings involved adjacent orthogonally-positioned PPs. They include, in reference to Figure 14, PP_{00}-PP_{01}, PP_{01}-PP_{02}, PP_{00}-PP_{10}, PP_{01}-PP_{11}, PP_{02}-PP_{12}, PP_{10}-PP_{11}, and PP_{11}-PP_{12}. The four remaining experiments involved diagonally oriented PP pairing PP_{00}-PP_{11}, PP_{01}-PP_{10}, PP_{01}-PP_{12}, PP_{02}-PP_{11}. Because of overlap in the PP pairings, some of the resistances are measured multiple times. For example, Rpv_{00}, Rpv_{02}, Rpv_{10} and Rpv_{12} are measured three times each while Rpv_{01} and Rpv_{11} are measured five times each. The same is true of the Rvs. Each of the eleven Rh values are computed only once, using Equation 10. The labels 'a' through 'k' are used to identify the Rh resistances (see Figure 14 for the labeling pattern).

A statistical plot illustrating the variations in the Rpv's is shown in Figure 15. The six groups of Rpv's are disseminated along the x-axis as a sequence of twenty-two vertical line plots. Each line plot contains twelve samples, one for each time the experiment was repeated. The variation in the values is illustrated as disper-

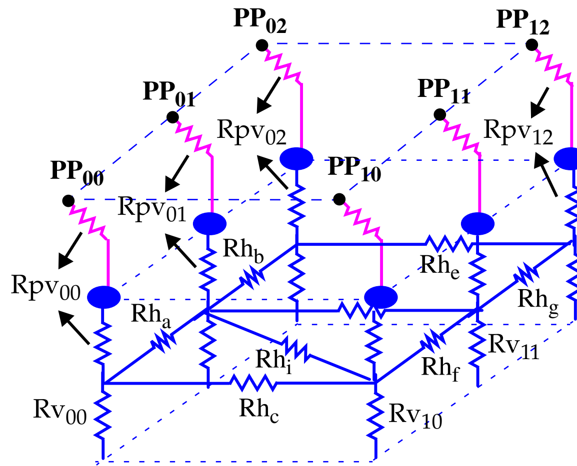

Figure 14. Resistance network on the test chips.

sion along the y-dimension in the graph. The mean and three σ limits are displayed as horizontal lines within each line plot.

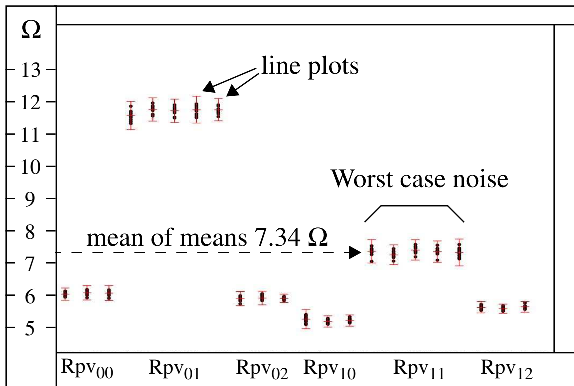

Figure 15. Noise Analysis of Rpv's

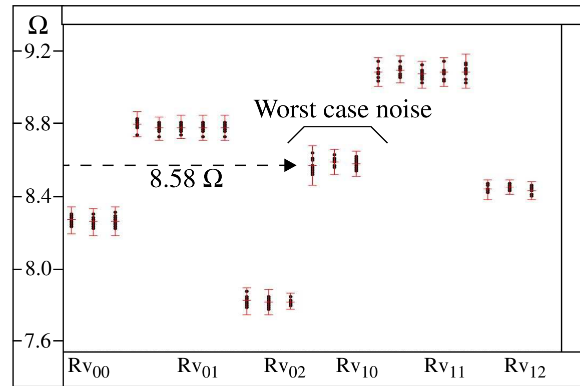

Figure 16. Noise Analysis of Rv's

The variation among the line plots within each of the groups as well as the variation within each line plot itself reflect the measurement resolution. This is true because, ideally, all of these points should have the same magnitude. The worst case fractional error is given for Rpv_{11} in which the largest 3 σ limit is 420 mΩs. The mean value is 7.34 Ω, which yields a 6% error.

The noise floor is smaller for the Rv's and Rh's. Figure 16 shows the mean and variance for the Rv's where the worst case variation is 120 mΩ for Rv_{10}. With a mean value of 8.58 Ωs, the fractional error in this case is 1.4% Similar results were obtained for the Rh analysis.

We indicated earlier that the magnitudes of the resistance elements in the PDS of our chips are larger than

those of a commercial product. The smaller resistances in a commercial grid impact the resistance resolution analysis reported here. For example, the voltage drop with RMC_{00} enabled is approximately 7 mVs in our chips. In contrast, Figure 6 gives simulation data for a model that better represents a commercial chip, and shows the voltage drop is approximately 2 mVs (3.5 times smaller). Since the precision of the voltmeter is unchanged, and the noise level is expected to be about the same, this suggests that our 6% maximum error could increase to 21% (6% x 3.5) for a commercial grid. However, the reduction in voltage drop is compensated for, in part, by the increase in current resolution. For example, the fraction of the total current drawn in our chips from PP_{00} with RMC_{00} enabled is 24% and the fraction increases to 44% in the model of the commercial grid. This factor of 1.8 partially compensates for the loss in voltage resolution. Based on this analysis, we expect the worst case error to be approximately 10% for a commercial grid[4].

IV. Analysis of Power Grid Resistance Variations

In this section, we apply our measurement technique to two sets of twelve chips and report the PDS resistances described in relation to Figure 14. The first chip set, CS_1, was fabricated early in the development of the 65 nm process. The second set, CS_2, was fabricated in the same process at a later time, and after improvements were made. Our analysis demonstrates that the proposed methodology can be used to measure and identify the major sources of process variations in the BEOL process steps.

A statistical analysis of the Rpv's for each set of chips, CS_1 and CS_2, is shown in Figures 17 and 18, respectively. Although the mean values are similar, the magnitude of the variation in resistance is larger for CS_1 than it is for CS_2 in four of the six cases. For example, the variation in Rpv_{01} for CS_1 is more than twice that of CS_2 and is well above the noise floor of 420 mΩs as shown in Figure 15. The extreme values in the line plots of this group suggests that resistance varies by almost 4 Ohms. The reverse trend occurs for Rpv_{02} and Rpv_{12}, however, i.e. the variation is larger for CS_2 than for CS_1. These are the only instances where this occurred in the entire analysis, and the root cause is difficult to determine without physical

[4]. We expect the error level can be reduced to less than 5% if more sophisticated instrumentation and noise reduction techniques are employed.

inspection. One possibility involves resistance variations in the packages, since the Rpv's include an off-chip Rp component.

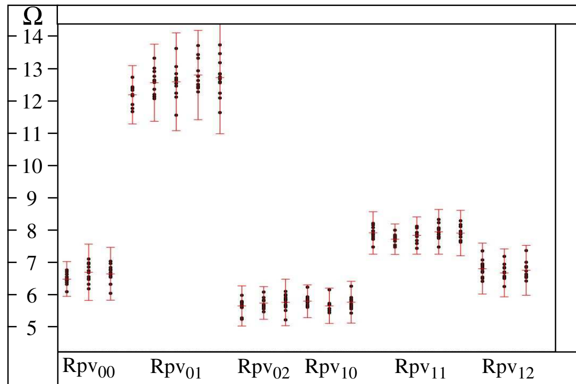

Figure 17. Rpv analysis for chip set 1 (CS1).

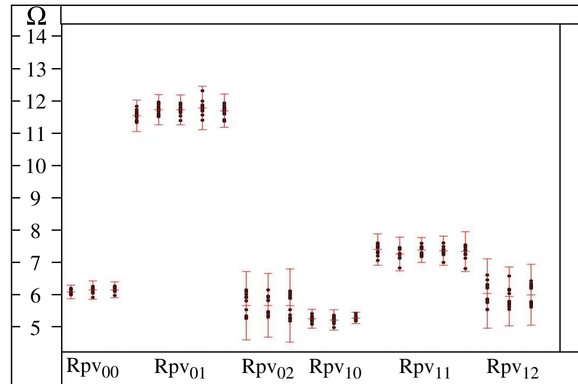

Figure 18. Rpv analysis for chip set 2 (CS2).

The most significant differences in variation between the two sets of chips occur in the Rvs. The line plots in Figures 19 and 20 display the results in a 3-D format. The mean values of the Rvs for CS_1 vary from 9.0 to 12.0 Ω while those for CS_2 vary from 7.8 to 8.0 Ω. The magnitude of the variation for the CS_1 Rv's is nearly three times that of the CS_2 Rv's. As noted above, the noise floor three σ limit is 120 mΩ, which is well below the variations observed in either plot. The worst case three σ variance for the CS_1 Rv's is 14.3 Ω in contrast to 2.01 Ω for the CS_2 Rv's.

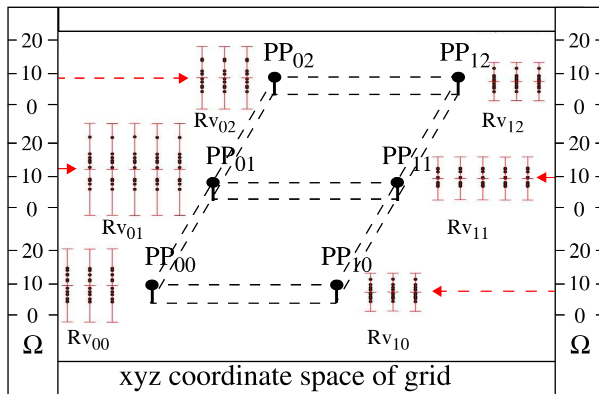

Figure 19. Rv analysis for CS_1.

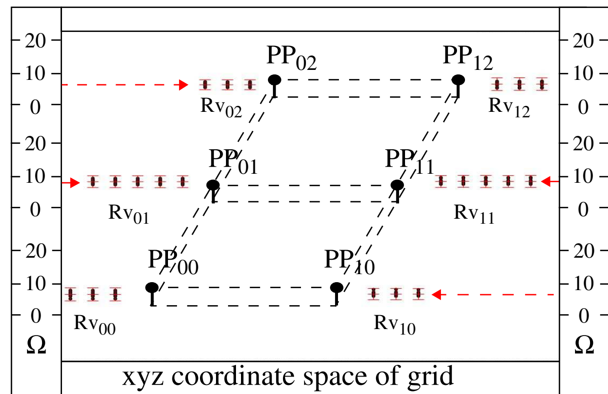

Figure 20. Rv analysis for CS_2.

In order to investigate the source of the Rv variation further, we ran a special set of experiments involving a set of 'alternative' RMCs shown in Figure 21, labeled as RMC$\mathbf{a}_{xy}$. These alternative RMCs are within 5 μm of the original set of RMCs shown as shaded boxes in Figure 21. The stimulus transistors in the original

set of RMCs were used in the three tests. However, the voltages were measured using the alternative RMCa's voltage sense transistors. The voltage profile shown in Figure 5 suggests that the resistances measured using the RMCa's reflect the characteristics of only the upper layers of the power grid[5]. If the variation measured from these tests is smaller than that shown in Figures 19 and 20, then it can be inferred that the main source of variation is in the lower layers of the power grid.

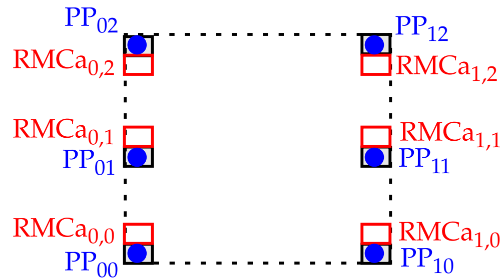

Figure 21. Alternative RMCs used in special experiments.

This is indeed the case as shown by the line plots of Figures 22 and 23, which illustrates that the magnitude of the variation is much smaller than that portrayed in Figures 19 and 20. (Note that the scale of the plots in Figures 22 and 23 is in the 100's of mΩ range). In contrast to Figures 19 and 20, only a small increase in variation is observable in the upper layers of CS_1 over CS_2. From this, we can infer that the main source of variation in the Rv's shown in Figure 19 is in the lower vias and wires.

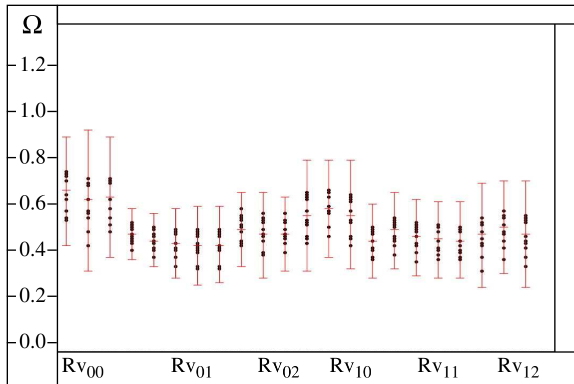

Figure 22. Adjacent RMC Rv analysis for CS_1.

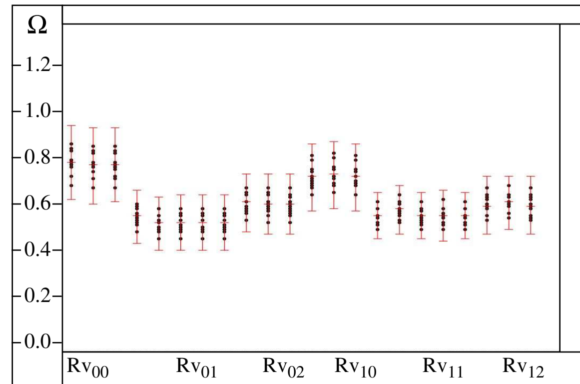

Figure 23. Adjacent RMC Rv analysis CS_2.

The variation in Rh is given by the line plots in Figures 24 and 25 for CS_1 and CS_2, respectively. The

[5] The infrastructure can be designed to enable all metal layers to be characterized in this fashion by routing a set of voltage sense wires to each of the metal layers.

magnitude of the variation in CS_2 is only slightly smaller than that for CS_1, which suggests the resistance per square remained fairly uniform in the two chip sets. Bear in mind that Rh primarily reflects the charac-

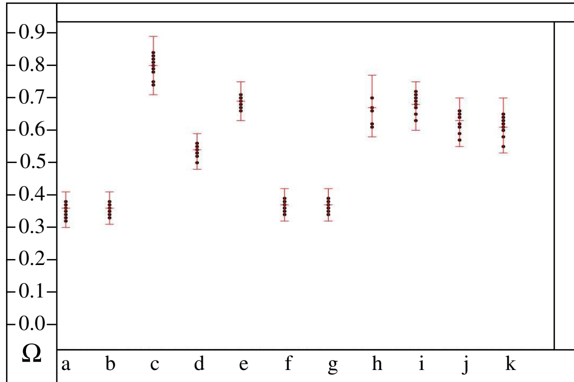

Figure 24. Rh analysis CS_1.

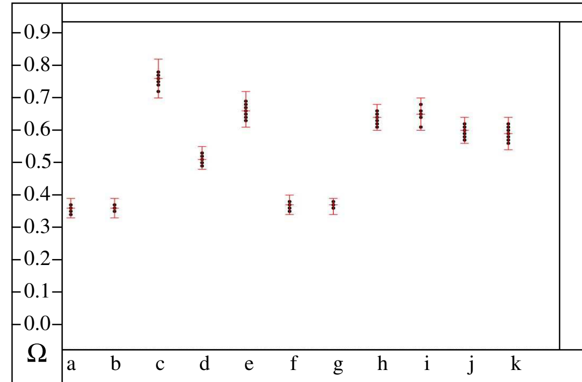

Figure 25. Rh analysis CS_2.

teristics of the top metal layers. Consequently, the lateral resistance of the lower metal layers cannot be measured directly using this approach[6].

V. Conclusion

The infrastructure proposed in this work can be used to characterize BEOL resistance variations during process bring-up and debug. It can also serve as a process monitor to track variations over time. The embedding of the infrastructure in the context of the actual circuit increases the relevance of the resistance analysis that it provides. The results of the analysis of resistance variations on two set of chips fabricated in a 65 nm technology illustrates that BEOL variations can be significant. The analysis enabled by the proposed infrastructure can help reduce delays in manufacturing development and yield learning cycle times caused by BEOL resistance variations.

Acknowledgements

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VI. References

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