A Process and Technology-Tolerant I_{DDQ} Method for IC Diagnosis

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Abstract

The use of I_{DDQ} test as a defect reliability screen has been widely used to improve device quality. However, the increase in subthreshold leakage currents in deep submicron technologies has made it difficult to set an absolute pass/fail threshold. Recent work has focused on strategies that calibrate for process and/or technology-related variation effects. In this paper, a new I_{DDQ} technique is proposed that is based on an extension of a V_{DDT}-based method called Transient Signal Analysis (TSA). The method, called Quiescent Signal Analysis or QSA, uses the I_{DDQ}s measured at multiple supply pins as a means of localizing defects. Increases in I_{DDQ} due to a defect are regionalized by the resistive element of the supply grid. Therefore, each supply pin sources a unique fraction of the total I_{DDQ} drawn by the defect. The method analyzes the regional I_{DDQ}s and "triangulates" the position of the defect to an (x,y) location in the layout. This information can be used in combination with fault dictionary-based techniques as a means of further resolving the defect's location.

1.0 Introduction

I_{DDQ} has been used extensively as a reliability screen for shorting defects in digital integrated circuits. Unfortunately, single threshold I_{DDQ} methods applied to devices fabricated in deep sub-micron technologies are resulting in unacceptably high levels of yield loss. The significant increase in subthreshold leakage currents in these technologies is making it difficult to set an absolute pass/fail threshold that fails only defective devices [1]. Several methods have been proposed as solutions to the subthreshold leakage current problem and, more recently, to process variation issues. Current signatures [2], delta-I_{DDQ} [3] and ratio-I_{DDQ} [4] are based on a "self-relative" analysis, in which the "average" I_{DDQ} of each device is factored into the pass/fail threshold value. In the following discussion, we will refer to the technology dependency of subthreshold leakage current as a *technology-related variation* effect to contrast it with the chip-to-chip variation effects caused by changes in process parameters (*process variation*).

The approach proposed in this paper is based on a previous V_{DDT}-based method called Transient Signal Analysis (TSA) [5]. TSA uses regression analysis to calibrate for process and technology-related variation effects by cross-correlating multiple supply pin transient signals measured under each test sequence. The I_{DDQ} method proposed in this paper, called Quiescent Signal Analysis or QSA, uses a set of I_{DDQ} measurements instead, each obtained from the individual supply pins of the Device-Under-Test (DUT). The process and technology calibration procedure used in QSA is based on the regression analysis procedure similar to TSA.

In TSA, we referred to signal variation resulting from defects as regional variation, to contrast it with the global variations introduced by process and technology-related effects. For transient signals, the supply rail's RC network modifies signal characteristics, such as phase and magnitude, at different supply pin test points. In QSA, only the resistive component of the supply rail network introduces variation in the I_{DDQ} values at different supply pins. In either case, the position of the defect in the layout with respect to any given power supply pin is related to the amount of regional "defect" variation observed at that pin. For QSA, the variation is directly related to the resistance between the defect site and the pin. For example, a larger value of I_{DDQ} is expected on supply pins closer to the defect site because of the smaller R. Therefore, the multiple I_{DDQ} measurements can be used to detect the defect as well as "triangulate" the physical position of the defect in the layout.

Defect detection experiments are on-going and will be addressed in a future work. In this work, a diagnostic method for QSA is developed and a set of simulation results are presented to demonstrate its defect localization accuracy. A characterization procedure is proposed that can be performed beforehand to determine the mapping between resistance and distance in the layout. Our results show that, on average, the (x,y) layout prediction given by the method is within 6% of the actual defect location in both 2μm and 0.25μm technologies. The worst case error is approximately 10%. This suggests that the technique is best used in combination with fault dictionary techniques as a means of further resolving the defect's location.

This paper is organized as follows. Section 2.0 describes related work. Section 3.0 presents the experimental design. Section 4.0 describes the method. Section 5.0 presents the results of experiments. Section 6.0 discusses the regression analysis technique that can be used to calibrate for process and technology-related variation effects. Section 7.0 provides a summary and conclusions.

2.0 Background

Several diagnostic methods have been developed based on I_{DDQ} measurements. In general, these methods produce a list of candidate faults from a set of observed tester fail-

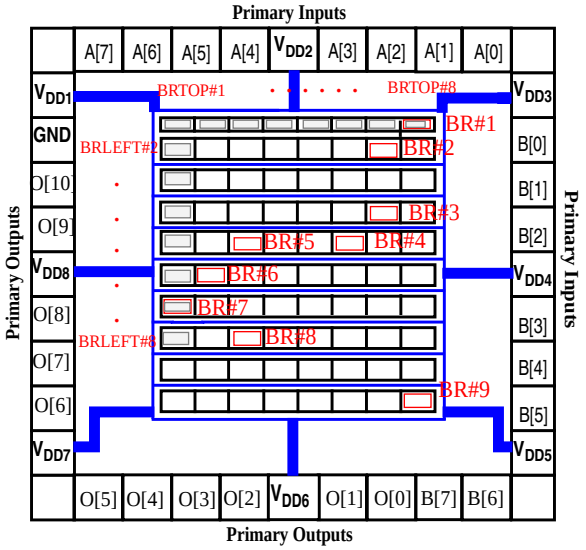

Figure 1. The layout of the 8-bit multiplier with resistive bridging defects.

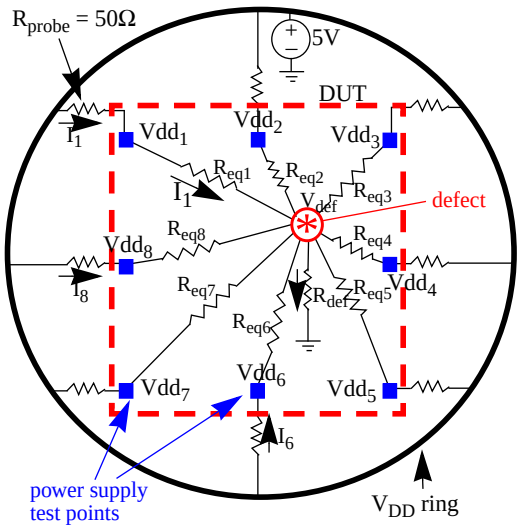

Figure 2. Equivalent resistance network with defect inside the circuit.

ures using a fault dictionary. The likelihood of each candidate fault can be determined by several statistical algorithms. For example, signature analysis uses the Dempster-Shafer theory, which is based on Bayesian statistics of subjective probability [6]. Delta I_{DDQ} makes use of the concepts of differential current probabilistic signatures and maximum likelihood estimation [7]. Although these methods are designed to improve the selection of fault candidates, in many cases, they are not able to generate a single candidate. Other difficulties of these methods include the effort involved in building the fault dictionary and the time required to generate the fault candidates from the large fault dictionary using device tester data.

The QSA procedure proposed here can help in the selection of the most likely candidate from the candidate list produced by these algorithms. The physical layout information generated by our method can be used with information that maps the logical faults in the candidate lists to devices in the layout. In addition, it may be possible to use the (x,y) location information provided by QSA as a means of reducing the search space for likely candidates in the original fault dictionary procedure. This can reduce the processing time and space requirements significantly.

3.0 Experimental Design

QSA experiments were conducted on a full-custom design of an 8-bit 2's complement multiplier. A block diagram of this device is shown in Figure 1. The primary inputs, labeled A[0] through A[7] and B[0] through B[7] are shown along the top and right of the figure. Only ten of the primary outputs are wired to the pad frame (and observable at the package pins of the device.) The power supplies for the core logic are labeled as V_{DD1} through V_{DD8} and are distributed evenly along the periphery of the core logic. The core logic consists of a rectangular array of AND gates and full adders, shown as rectangles in the center of the figure. Resistive bridging (Figure 1) and open (not shown) defects were inserted into these cells at the labeled locations in the figure. 9 of the bridging defects and the open defects were distributed throughout the layout. 15 additional bridging defects were placed in cells along the top and left sides. The SPACE extraction tool was used to generate RC models from the layout [8].

4.0 Experimental Method

In this section, we describe the QSA technique used for localizing shorting defects. Since the simulations models did not allow for significant background currents, they are not accounted for directly in this section. However, Section 6.0 describes several extensions of the method that "calibrate" for the significant leakage currents associated with current technologies.

The method is composed of two phases: Resistance Network Analysis and Resistance-to-Distance Analysis.

- **Phase 1: Resistance Network Analysis**

The objective of this phase is to determine the "equivalent resistance" (R_{eq}) between each of the supply pads and the point from which the defect draws current from the supply grid. The R_{eq} are labeled R_{eq1} through R_{eq8} in Figure 2. The R_{eq} are computed by setting the state of the circuit such that the short is provoked and the voltages at each of the supply pads is measured. Under this condition, the defect will draw current from each of the supply pads proportional to the value of the R_{eq}. The 50 Ohm resistor (R_{probe} in Figure 2) placed in series with the supply pad probes allows the currents to be measured as voltage drops in these experiments. If the appropriate measurement instrumentation is available, I_1 through I_8 can be obtained directly without the use of these resistors.

Figure 3 shows the supply pad voltages from a simula-

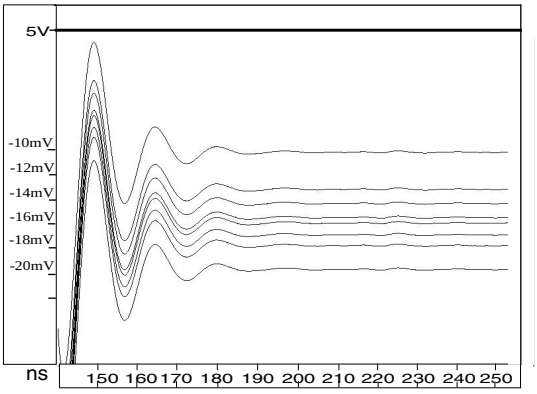

Figure 3. .Voltage waveforms measured at the eight supply pins with the shorting defect provoked.

tion of a device with a defect inserted at the location shown in Figure 2. The vertical displacement of the waveforms along the right portion of the figure indicate that the defect causes a regional current variation in the device. The magnitude of the voltage drop (from V_{DD}) of each of the waveforms in Figure 3 is inversely related to the R_{eq} between the supply pads and the defect site. Therefore, the supply pads with the largest voltage drops indicate they are in close proximity to the defect. Although it is unlikely that the relationship between R and distance is strictly linear and uniform along all directions from the supply pads to points in the layout, it is certainly valid to assume it approaches such a function if the supply topology is grid-like and regular. We will show that good results are obtained under this assumption for our experimental circuit. A procedure for dealing with irregular topologies is proposed in the next section.

Since the I_{DDQ} values are related only to the resistive components of the network as shown in Figure 2, the following system of equations can be written to describe its behavior. The I_i variable represents the branch currents

$$I_i \times (R_{eqi} + R_{probe}) = V_{def} \quad \text{for i = 1 ... 8}$$
$$\text{i = 1 ... 8}$$

Equation 1. System of equations

through each of the supply pins, R_{probe} is known (50 Ohms in our experiments), and R_{eqi} are the unknowns. The voltage at the defect site (V_{def} at the "star" in the figure) is also unknown but can be used as the point of reference for the system of equations. This formulation yields 8 equations and 9 unknowns. Therefore, without additional information, we cannot solve for the R_{eqi}. However, the important information is the *relative differences* between the R_{eqi} and not their absolute values. This relationship is captured by computing ratios. As described in the next section, the ratios can be scaled as easily as the real Rs to obtain the location of the defect. The ratios of the resistances R_{eq1} to R_{eq8} are computed from the equations given in Equation 2 below.

$$I_i \times (R_{eqi} + R_{probe}) = I_k \times (R_{eqk} + R_{probe})$$
$$R_{ratioi} = \frac{I_j}{I_i} \times R_{eqj} + \left(\frac{I_j}{I_i} - 1\right) \times R_{probe}$$
$$\text{for i = 1 ... 8 excluding j}$$

Equation 2. Resistance ratios of R_1 to R_8

These equations express 7 of the R_{eqi} as a function of the 8th. The R_{eqj} for the pad that has the maximum current value I_k is chosen as the reference resistance.

- **Phase 2: Resistance-to-Distance Analysis**

The objective of this phase is to map from the $R_{ratiosi}$s to a set of distances in the layout, each directed from a supply pad to the defect site. In the ideal case, the resistance ratios scale linearly to distance uniformly along any vector. However, complex and/or irregular supply topologies routed in multiple levels of metal with resistive contacts connecting them, can complicate the resistance to distance mapping function. Two mapping functions are described; one the assumes linearity and a second that handles more complex supply rail topologies.

i) Method 1:

This method simply uses the resistance ratios as distance ratios, which are scaled by a common factor as a means of finding a point of intersection among them. The following steps summarize the process and its heuristics:

Step 1 Select the V_{DD} supply pad, V_{DDk}, closest to the defect site. This is equivalent to selecting the largest current value, I_k or the minimum resistance, R_{eqk} in Equation 2. Since d_k is assumed proportional to R_{eqk}, V_{DDk} is closest and is referred to as the primary supply pad.

Step 2 Select the two supply pads adjacent to the primary supply pad. If the supply pad configuration is similar to the one shown in Figure 1, it is possible that these choices result in a line of pads along one dimension of the layout. For example, if the supply pads V_{DD3}, V_{DD4} and V_{DD5} are selected in the design shown in Figure 1, only the y dimension is "covered". In this case, the supply pad adjacent to the first two in the other dimension is selected (e.g. V_{DD2} since it "covers" the x dimension). Similar heuristics can be used for other supply pad configurations.

Step 3 Using the three selected supply pads, establish a set of circles with radii proportional to the ratios computed in Equation 2. The simple algorithm is used to iteratively scale the radii by the same factor and tests for intersection. The point of intersection indicates the (x,y) location in the layout at

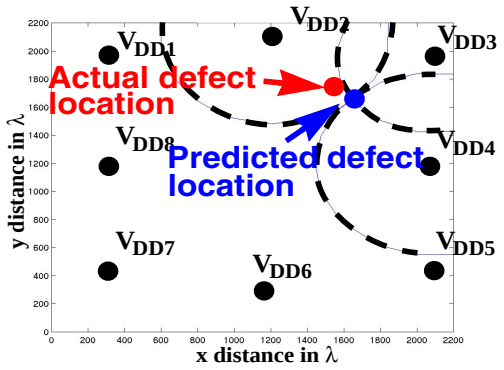

Figure 4. Bridging Experiment #1 using localization Method 1.

which the defect draws current from the supply grid.

An application of this method is shown in Figure 4 for Bridging Experiment #1. The figure represents the layout of the multiplier with the x and y scales given in units of lambda. The supply pad locations are shown as "stars" along the edges of the figure. Three dashed circles are shown in the upper right hand corner centered around the supply pads V_{DD2}, V_{DD3} and V_{DD4}. These supply pads were selected because they are adjacent, as given in Steps 1 and 2 in the method. The circles have been scaled so that they have a common point of intersection. The predicted and actual (x,y) locations are given by "star"s in the figure.

ii) Method 2:

The second method uses a contour to map resistance to distance in the layout. Since the actual mapping function is not easily obtained, this estimate is designed to provide a more accurate prediction for supply grid designs with irregular topologies. The data to construct the contour can be obtained easily using a defect-free device or a simulation model.

The method additionally uses the equivalent R_{eq} between the supply pads. They can be obtained between each pairing of supply pads by setting the supply pad under test to a voltage slightly less (e.g. 100mV) than the nominal supply voltage. The remaining supply pads are set to their nominal voltage and the currents measured. The distance between each pairing of supply pads is easily obtained from the layout. The ratio of distance and resistance defines the scaling factor along each of the vectored directions from the supply pad under test to the other supply pads. The experiments produce a set of contours (one for each supply pad) that are used instead of the circles in the localization procedure described for Method 1.

This method simulates the presence of a defect at each of the supply pads. Therefore, the R_{eq} obtained from the measurement accurately reflects the R for defects in the vicinity of that supply pad. The drawback of contours is

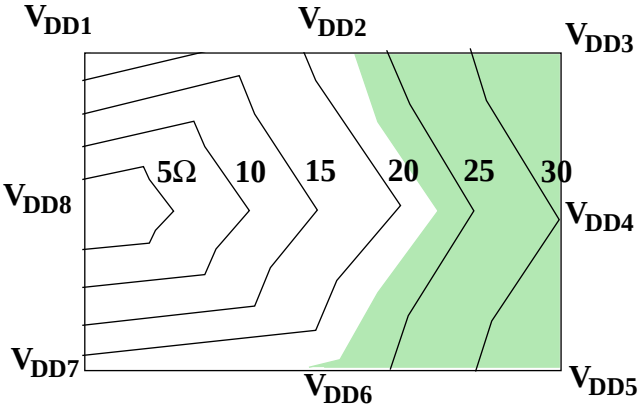

Figure 5. The resistance-to-distance mapping contour for V_{DD1}.

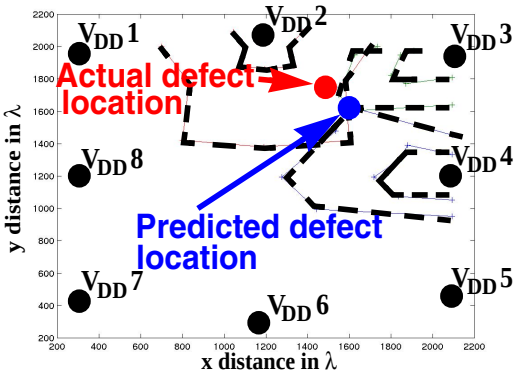

Figure 6. Bridging Experiment #1 localization using contour maps (Method 2).

that they may produce several different points of intersection under different scaling factors. Therefore, several predicted locations may be generated by the algorithm described in Method 1 above.

Figure 5 shows the contour obtained for V_{DD8} in our experiments. The lines representing the contour are each labeled with the R_{eq} they define at points in the layout under their curve. A full set of contours would consist of one such mapping for each supply pin. Figure 6 shows the method applied to the resistance data obtained for Bridging Experiment #1. In comparison to the localization result shown in Figure 4, only slightly better results are obtained for this experiment using contour maps.

5.0 Experimental Results

The errors between the actual and predicted locations of the defects (columns 2, 3, 5 and 6) are presented for the bridging and open experiments in Table 1. The error is computed using the following expression: $\frac{\sqrt{(x_{predicted}-x_{actual})^2+(y_{predicted}-y_{actual})^2}}{\text{width\_of\_layout}} \times 100$ in which the width of the layout is 2,200 lambda. Only 3 of

Table 1: Experimental Results

Defect	%Err 2μm	%Err .25μm	Defect	%Err 2μm	%Err .25μm
BR#1	6.3%	5.11%	BRtop#1	1.8%	7.58%
BR#2	7.1%	5.42%	BRtop#2	4.4%	4.54%
BR#3	9.9%	2.41%	BRtop#3	6.8%	2.54%
BR#4	6.5%	3.89%	BRtop#4	3.87%	4.12%
BR#5	2.6%	6.85%	BRtop#5	1.94%	6.83%
BR#6	7.1%	10.17%	BRtop#6	8.45%	3.70%
BR#7	9.5%	3.61%	BRtop#7	5.3%	2.79%
BR#8	3.6%	7.73%	BRtop#8	2.38%	5.39%
BR#9	5.9%	5.40%	BRleft#2	0.82%	6.99%
OP#3	9.1%	4.09%	BRleft#3	3.5%	5.9%
OP#7	9.86%	3.97%	BRleft#4	5.8%	6.63%
OP#9	7.65%	3.41%	BRleft#5	7.3%	8.39%
			BRleft#6	5.45%	8.19%
			BRleft#7	9.58%	5.14%
			BRleft#8	5.53%	3.44%

the 9 open defects were diagnosable because the floating node under experiments OP#3, OP#7 and OP#9 caused a shorting condition between V_{DD} and GND in downstream gates.

Columns 2 and 3 of Table 1 indicate the worst case error is 10.17% for BR#6 while the mean error in either technologies is about 6%. We expect that inaccuracies in the extracted model and simulation tolerances are responsible for a portion of this error. However, the average distance from the actual defect site to the point at which the defect draws current from the supply rail is approximately 50 lambda. This accounts for approximately 2.5% of the prediction errors tabulated in Table 1.

6.0 Process Variation and Leakage Current

The background leakage currents measured in the simulation experiments (< 30nA) were very small. However, in deep sub-micron technologies, these currents are orders of magnitude higher and must be accounted for. In this section, we describe a regression analysis procedure for QSA that can be used to calibrate for background currents. The method is adapted from the procedure defined for TSA [5].

The defective device I_{DDQ} consists of two components, the current drawn by the defect, and the process and technology-related leakage current, e.g. subthreshold leakage current. This changes the formulation presented in Equation 2 to that shown in Equation 3 below.

The leakage current is given as a set of currents, $I_{leakagei}$ in the equations, each representing the current drawn

$$(I_{leakagei} + I_{defecti}) \cdot (R_{eqi} + R_{probe}) = (I_{leakagek} + I_{defectk}) \cdot (R_{eqk} + R_{probe})$$

Equation 3. Equation 2 reformulated with background current

through each of the supply pins. If the transistor density in the layout is regular, then the leakage current will be evenly distributed among the supply pins yielding a single value for $I_{leakagei}$. However, if the transistor density in the layout varies across the design, then the $I_{leakagei}$ will also vary in each supply pin since the supply rail will distribute the current proportionally as a function of its resistance. The "localized" variation of the leakage current will adversely affect the localization methods described in the previous section unless it is accounted for.

The key observation concerning leakage current is that it is effected most significantly by the "global" variations introduced by changes in process and technology-related parameters. In other words, the current variations introduced by variations in these parameters will affect all transistors and junctions in a device in a similar manner. We are not claiming that intra-device variations do not exist, but rather that they are smaller in magnitude and can be ignored. The more significant global variations will scale the leakage currents in all supply rails proportionally, making it possible to track it using regression analysis.

A graphical representation of leakage current tracking behavior is shown in Figure 7. The x axis plots I_{DDQ} for supply pin k while the y axis plots it for supply pin i. The labeled points A through F represent measured values on these two pins from a set of defect-free devices. As noted in the figure, the pairs of I_{DDQ}s from each device track each other, e.g., changes in one value are matched by changes in the other value. The correlation in these pairings is tracked by the regression line (best fit line) shown in the figure. Unmodeled factors such as intra-device process variation and noise will make these data points non-colinear. Therefore, 3 sigma prediction limits are used to delimit a region around the line (labeled Process Variation Zone). In contrast, the "regional" variation caused by an active shorting defect will disrupt the correlation between the I_{DDQ}s as shown by data point G in the figure.

From Equation 3, it is clear that the system of equations is solvable (in the fashion described in Section 4.0) if the $I_{leakagei}$ are known quantities. Although several alternatives are possible, a method that accounts for vector-to-vector as well as chip-to-chip I_{DDQ} variations is expected to generate the best result. One way of accomplishing this is to assume that all of the current in the supply pin with the smallest I_{DDQ} is due to leakage. This I_{DDQ} can then be used to derive the leakage components in the other supply pins using the scatterplots derived from defect-free devices.

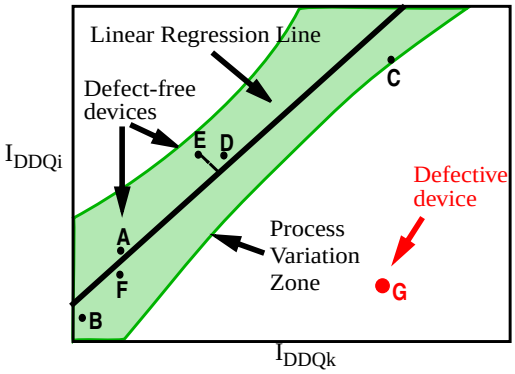

Figure 7. Scatter plot to determine the ratios between each two test points in defect free devices

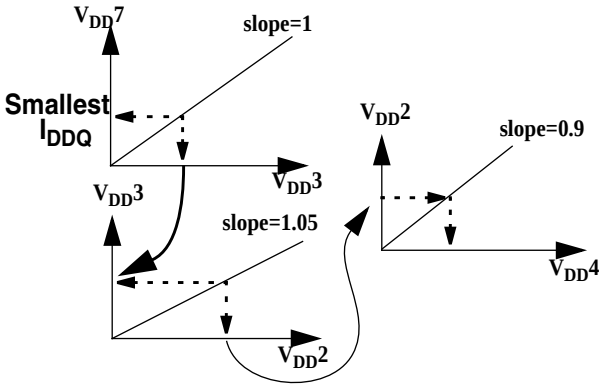

Figure 8. $I_{leakage}$ calibration using backward mapping across scatterplots.

The method is illustrated in Figure 8, in which the three scatterplots show the relationship of the leakage currents between four supply pads for some design. In this case, I_{DDQ7} is smallest and is used in a backward mapping procedure to obtain the leakage currents for I_{DDQ3}, I_{DDQ2} and I_{DD4}, as shown by the arrows in the figure. Note that slopes other than 1 in the regression lines indicate differences in transistor density across the layout, as described previously. The $I_{leakagei}$ obtained using this procedure can then be plugged into the equations given in Equation 3 and solved in a manner similar to that proposed for Equation 2.

7.0 Summary and Conclusions

In the paper, we describe a method based on the analysis of multiple power supply pin I_{DDQ} values for the localization of defects. The technique, which is called Quiescent Signal Analysis (QSA), consists of two phases. In the first phase, the relative values of the individual supply pin I_{DDQ}s are used as a means of determining the "equivalent" resistance between each supply pin and the defect site. In the second phase, a mapping function that relates resistances to positions in the layout is used to predict the location of the defect. Several calibration procedures are proposed for process and technology-related leakage currents that are based on linear regression analysis.

A set of simulation experiments were conducted on defective versions of an 8-bit multiplier circuit to demonstrate the method and its accuracy. The results of the experiments show that it is possible to predict the actual location of the defects within an error bound of 10%. Although better results are expected as the accuracy of the extracted model is improved, this technique is best used in combination with fault dictionary-based techniques as a means of further resolving the defect's location.

With respect to a hardware implementation of the technique, our main concerns are related to instrumentation accuracy. The simulation results of the device in 2.0um technology indicate that the ratio between the resistance of the defect network to ground to the "equivalent" resistances (from the supply pin to the defect site) are on the order of 200 to 1. In other words, a defect that draws 1mA current will produce I_{DDQ} variations in each supply pin in the 10's of uA range. If the measurement instrumentation is capable of distinguishing between values in that range, then good defect localization accuracy is expected. Technology trends and a better extraction procedure may reduce this ratio in more advanced technologies, further improving the accuracy of the method.

Simulations and hardware experiments are underway to investigate other aspects of the QSA procedure. Among these include experiments designed to test the process calibration techniques proposed in section 6.0. The defect detection capabilities of the method will be evaluated in the course of the research.

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