Midterm ECE 443

Name:

This exam has 10 questions

You must show all of your work -- partial credit may be given to partially correct answers, while answers with no justification may not receive full points. Use the back of the exam sheets if you need extra space.

WARNING: KEEP YOUR EYES ON YOUR OWN PAPER. CHEATING OF ANY SORT WILL CAUSE YOU TO FAIL THIS COURSE.

1) (10 pts) Write the **entity** description for the following schematic
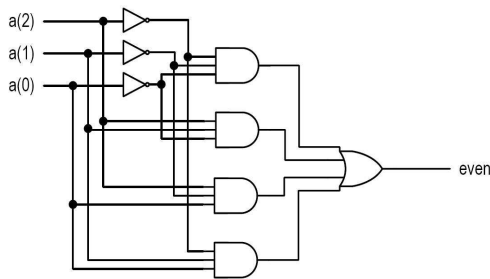
Input:
　a(2), a(1), a(0)

Output:
　even

a(2)	a(1)	a(0)	even
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

SOP expr: $even = a(2)' \cdot a(1)' \cdot a(0)' + a(2)' \cdot a(1) \cdot a(0) + a(2) \cdot a(1)' \cdot a(0) + a(2) \cdot a(1) \cdot a(0)'$

2) (10 pts) Briefly give the 3 rules for ensuring that a process block describes combinational logic.

3) (10 pts) **List** the three steps in ISE that translate a VHDL description to a bit-file for uploading to the FPGA. Three short phases will do.

4) (10 pts) Write the statement needed to assign the decimal value 5 to an unsigned signal *u1* declared as follows:

```
signal u1: unsigned(3 downto 0);
```

5) (10 pts) Draw the schematic for the following simple signal assignment statement (use boxes with a '+' sign for the adder(s)/subtractor(s)):

```
arith_out <= a + b + c - 1;
```

6) (10 pts) Would you use a *conditional signal assignment* or a *selected signal assignment* statement in a situation where you need a MUX?

7) (10 pts) Write a conditional signal assignment statement that implements the following function:

input	output	
r	code	active
1 – – –	11	1
0 1 – –	10	1
0 0 1 –	01	1
0 0 0 1	00	1
0 0 0 0	00	0

8) (10 pts) Simplify the following code segment, i.e., what is it equivalent to?

```
process(a, b, c, d)
  begin
  y <= a or c;
  y <= a and b;
  y <= c and d;
end process;
```

9) (10 pts) Write the architecture for a D FF with Asynchronous Reset given the following entity declaration:

```vhdl
library ieee;
use ieee.std_logic_1164.all;
entity dffr is
   port(
      clk: in std_logic;
      reset: in std_logic;
      d: in std_logic;
      q: out std_logic
   );
end dffr;

architecture arch of dffr is
   begin




end arch;
```

10) (10 pts) Write the VHDL code that implements the following RTL schematic