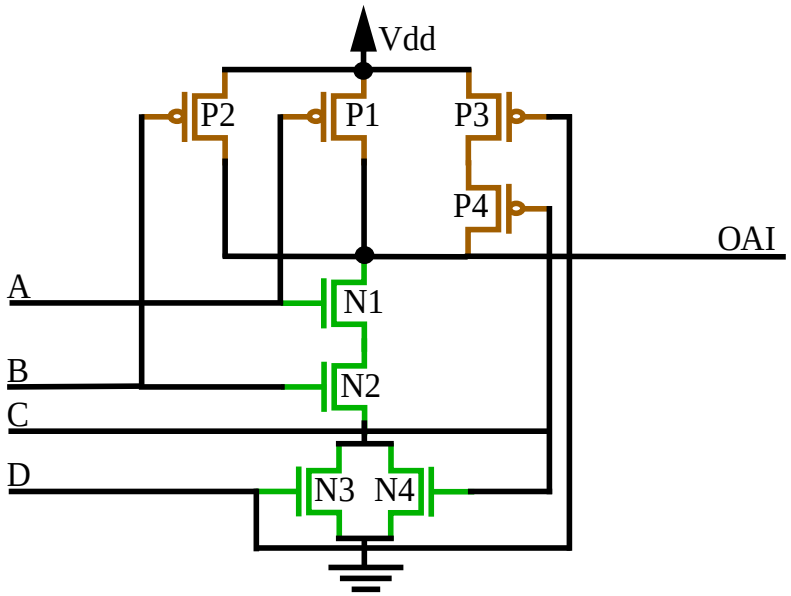
LAB Assignment #2 for CMPE 413/CMSC 711

Assigned: Wednesday, Sept 15th
Due: Wednesday, Sept 22th

Description: Create a compact layout for the following 2 gates:

- The OAI gate given in the schematic diagram below:



- The minimim implementation of either the XOR or XNOR gates that we discussed in class. Minimal implementation refers to the XOR and XNOR gates that do NOT use the inputs as sources for the output (pass-gate versions) and do NOT require complemented input literals.

- There are help documents on building contacts and on the layout editor Virtuoso on my web page. You must design these gates using AMI's 1.6um technology. The help documents will show you the steps involved in selecting this technology.

Report Requirements:

1) You will be graded on the compactness of the layout. Chintan and I will also do this assignment. We will compute the areas (W*L) of our designs and use those values as the benchmarks.
2) Generate a printout of the layouts (black-and-white is fine).
3) Include labeled transistor-level schematic diagrams (hand-drawn or word processor versions are okay) for the gates.
4) Grading will be based on the completeness of your write-up as well as the compactness of the layout. Laboratory writeups should be designed to allow others to recreate your work.