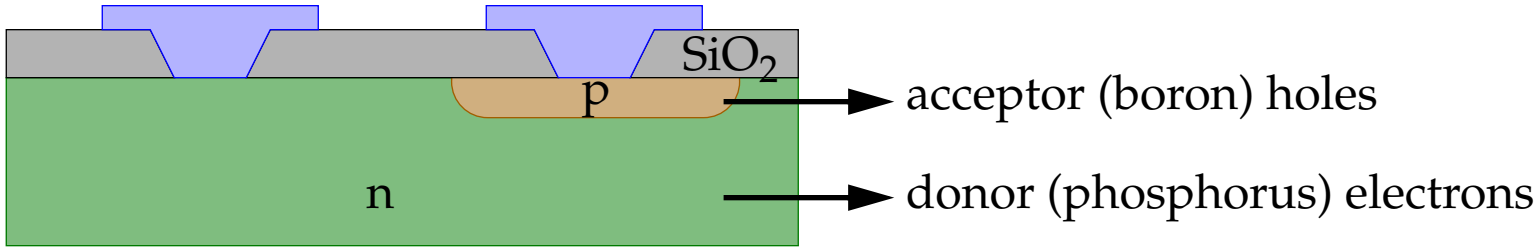
Physical Representation



Abrupt junction between *p* and *n* materials creates a concentration gradient among the carriers.

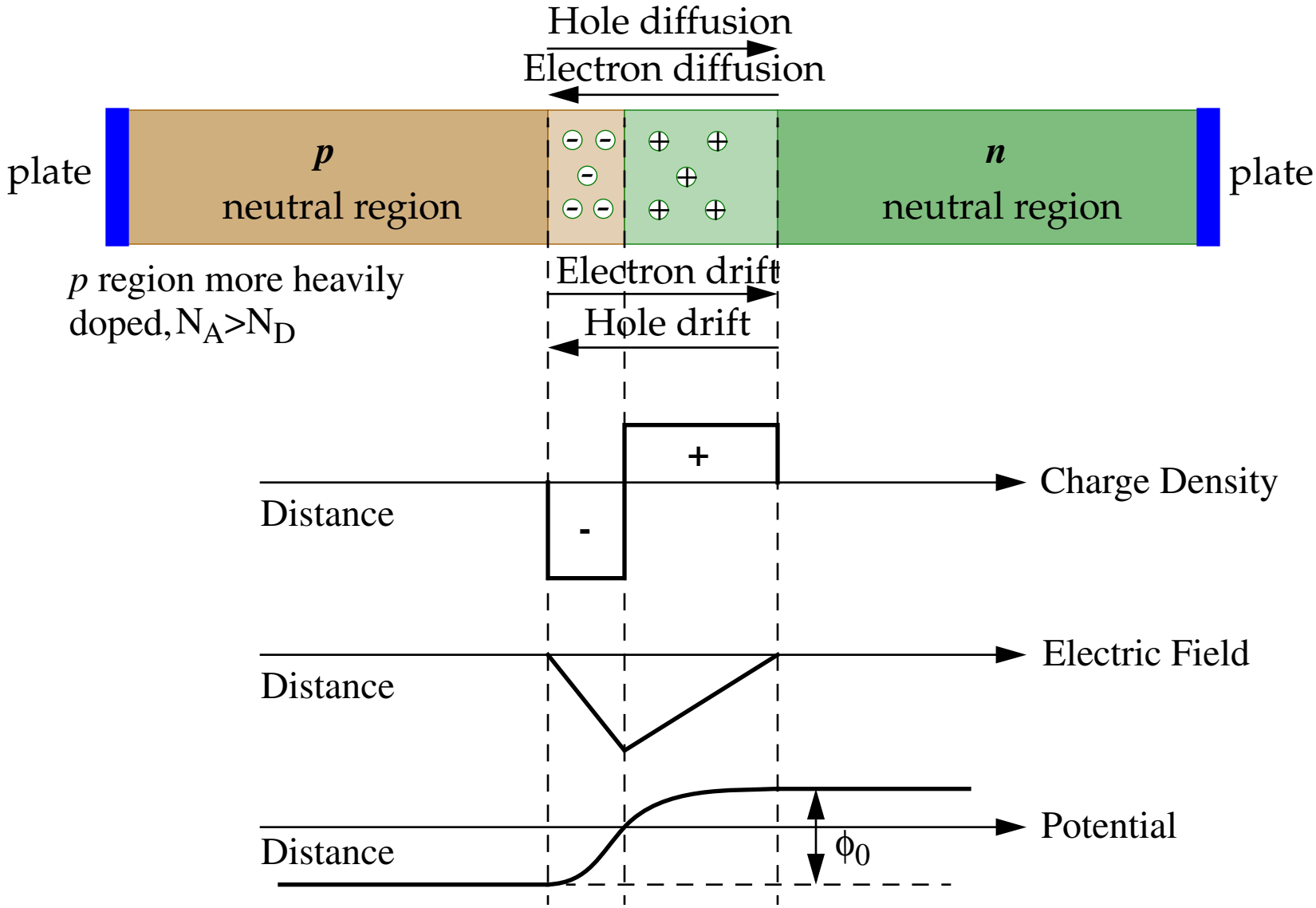
Electrons **diffuse** from *n* to *p* while holes diffuse from *p* to *n*.

The diffusion leaves behind *bound charge* in the lattice.

The bound charge sets up an electric field that counteracts the diffusion.

Electrons **drift** from *p* to *n* while holes drift from *n* to *p*.

Charge Distribution, Electric Field and Electrostatic Potential



Built-In Potential and I-V Characteristics

Build-in potential:

$$\phi_0 = \phi_T \ln\left[\frac{N_A N_D}{n_i^2}\right] \quad \text{where } \phi_T = \frac{kT}{q} = 26\text{mV at 300K (Thermal V)}$$

$$n_i = 1.5\times10^{10}\text{carriers/cm}^3$$

For example:

$$N_A = 10^{15}\text{carriers/cm}^3$$

$$N_D = 10^{16}\text{carriers/cm}^3$$

$$\phi_0 = 26\ln\left[\frac{10^{15}10^{16}}{2.25\times10^{20}}\right] = 638mV$$

Forward bias:

Raising potential of the *p* w.r.t *n* causes current to flow from *p* to *n*.

Lowers potential barrier and *diffusion* dominates *drift*.

Minority carriers injected into neutral region and diffuse toward plates.
Recombine with majority carrier causing a net flow of current.

I-V Characteristics

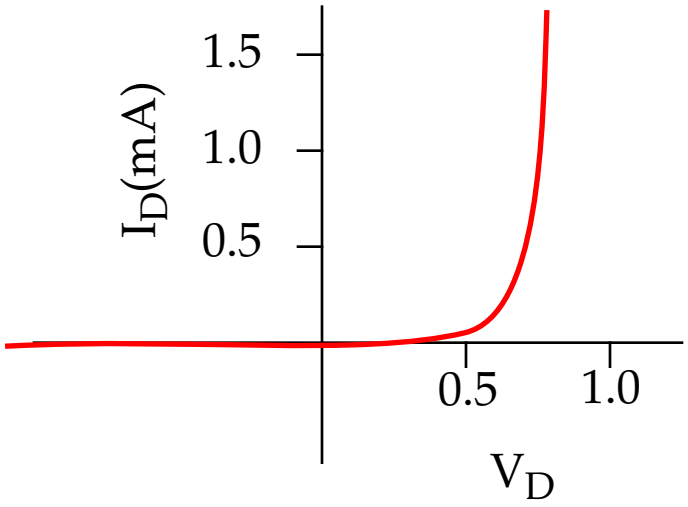
Reverse bias:

Raising potential of the *n* w.r.t *p* causes current to fl ow from *n* to *p*.

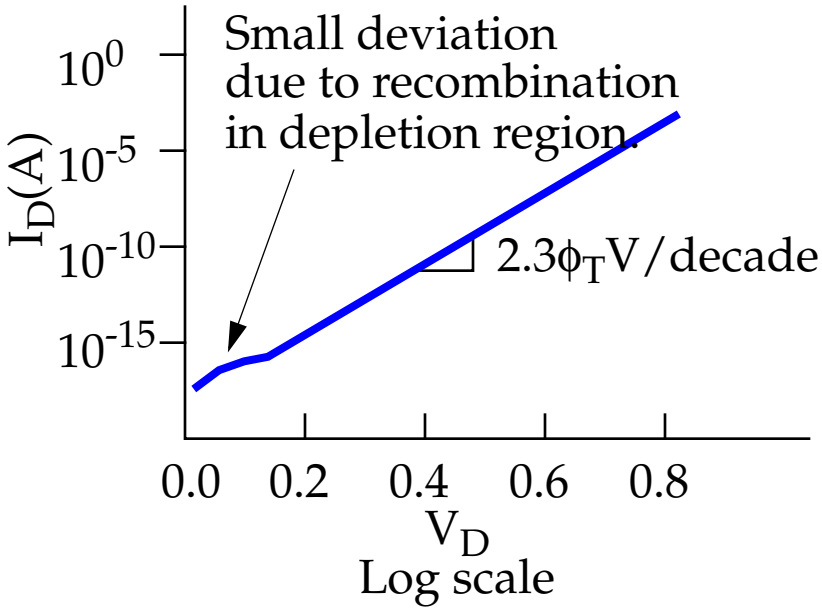
Drift dominates *diffusion*.

However, current is small since the number of minority carriers (e.g., electrons in *p* neutral region) is small.

For forward bias, the current is **exponentially** related to applied bias.



Linear scale



Log scale

Current increases by a factor of 10 for every 60mV ($2.3\phi_T$) of forward bias.

Static Behavior

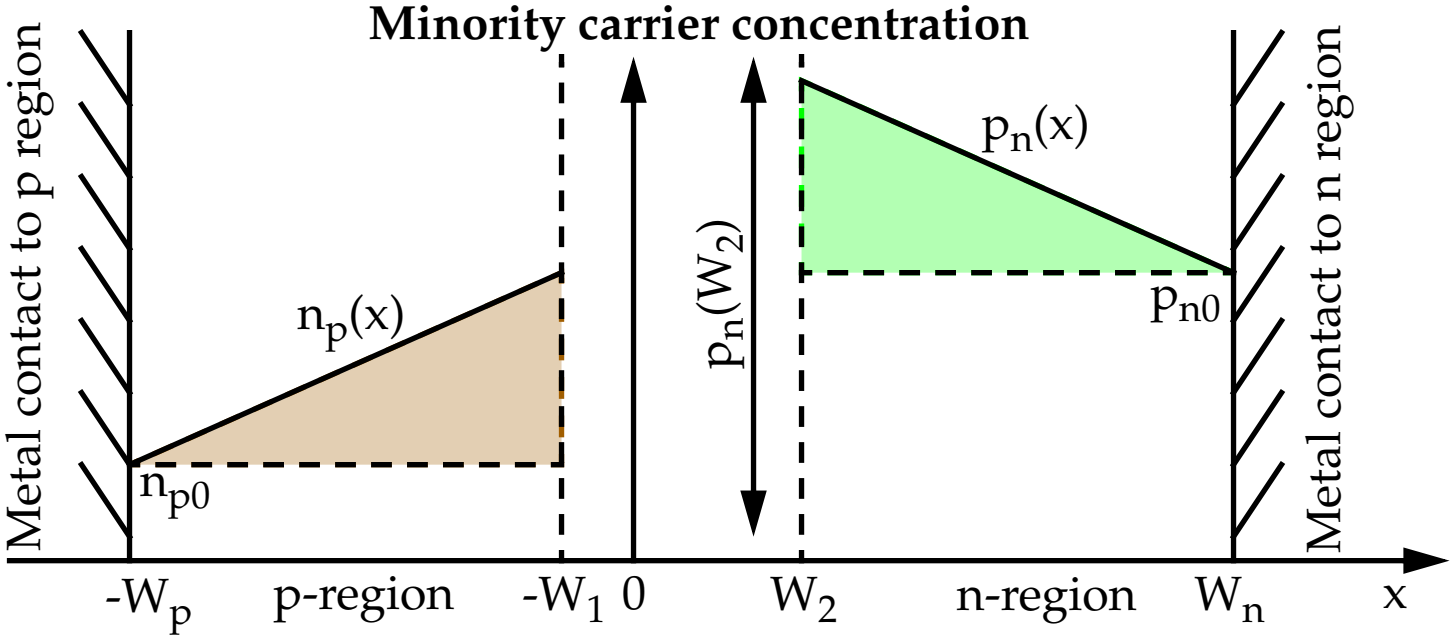
Ideal diode equation:

$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$ where I_S is a constant: saturation current.

With $V_D << 0$,

$I_D \sim= -I_S = 10^{-17} A/um^2$ (actual values are 10^3 higher)

Forward Bias: Physical basis for ideal equation:



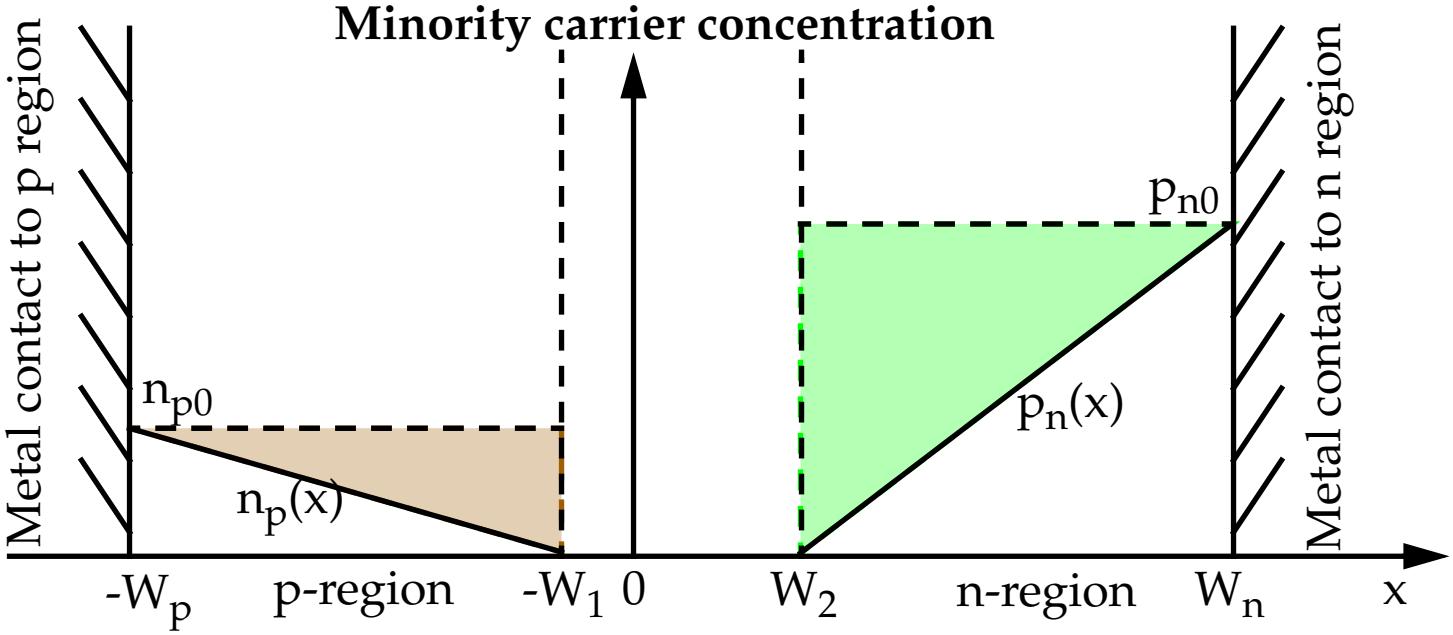
Static Behavior

Reverse Bias:

Ideal diode equation predicts diode current approaches the saturation current as V_D gets much *smaller* than the thermal voltage.

$$I_D \to -I_S \quad \text{for} \quad |V_D| \gg \phi_T$$

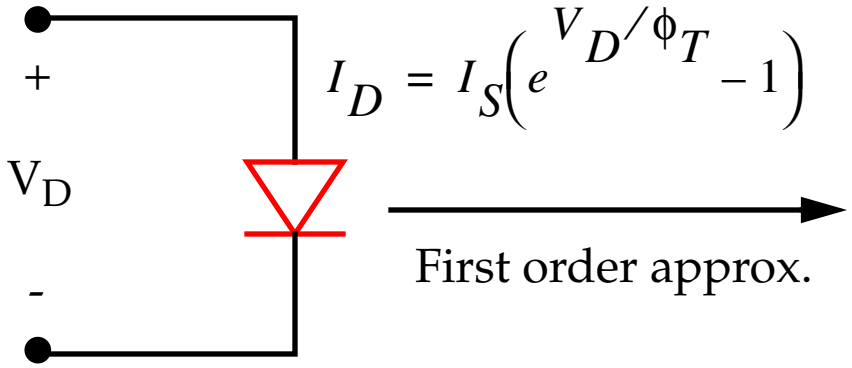
Concentration of minority carriers at depletion-region approaches 0 under sufficient reverse bias.



Static Behavior

Simple models of the diode.

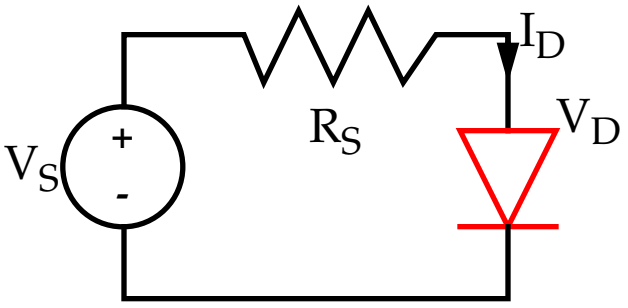
Left model based on ideal diode but is strongly non-linear and approximated by a simple model on the right.



Ideal diode model

For a fully conducting diode, voltage drop across diode is ~0.7V

Example: Assume V_S = 3V and R_S = 10kΩ and I_S = 0.5X10$^{-16.}$



Using non-linear model yields:
V_D =0.757V and I_D =0.224mA

Assuming V_D =0.7V yields I_D =0.23mA

Dynamic Behavior

Dynamic behavior determines the maximum operational frequency.

It is dependent on how fast charge can be moved around.

Two capacitances:

Depletion and *diffusion*.

Depletion region and *Junction* capacitance:

Under the ideal model, the depletion region is void of mobile carriers.

Its charge is determined by the immobile donor and acceptor ions.

Intuitively:

Forward bias: Potential barrier is reduced which means that *less* **space charge** is needed to produce the potential difference.

This corresponds to a *reduced* depletion-region width.

Reverse bias: Potential barrier increased, increase in space charge, *wider* depletion width.

Dynamic Behavior

Expressions that convey this fact.

- *Depletion region charge* (V_D is positive for forward bias):

$$Q_j = A_D\sqrt{2\varepsilon_{si}q\left(\frac{N_A N_D}{N_A + N_D}\right)(\phi_0 - V_D)} \qquad (1)$$

- *Depletion-region width*:

$$W_j = W_2 - W_1 = \sqrt{\left(\frac{2\varepsilon_{si}}{q}\frac{N_A + N_D}{N_A N_D}\right)(\phi_0 - V_D)} \qquad (2)$$

- *Maximum electric field*:

$$E_j = \sqrt{\left(\frac{2q}{\varepsilon_{si}}\frac{N_A N_D}{N_A + N_D}\right)(\phi_0 - V_D)}$$

where

$$\varepsilon_{si} = 11.7 \times 1.053\times10^{-12}\text{F/cm}$$

The ratio of the n-side versus p-side depletion region width is determined by the doping level ratios:

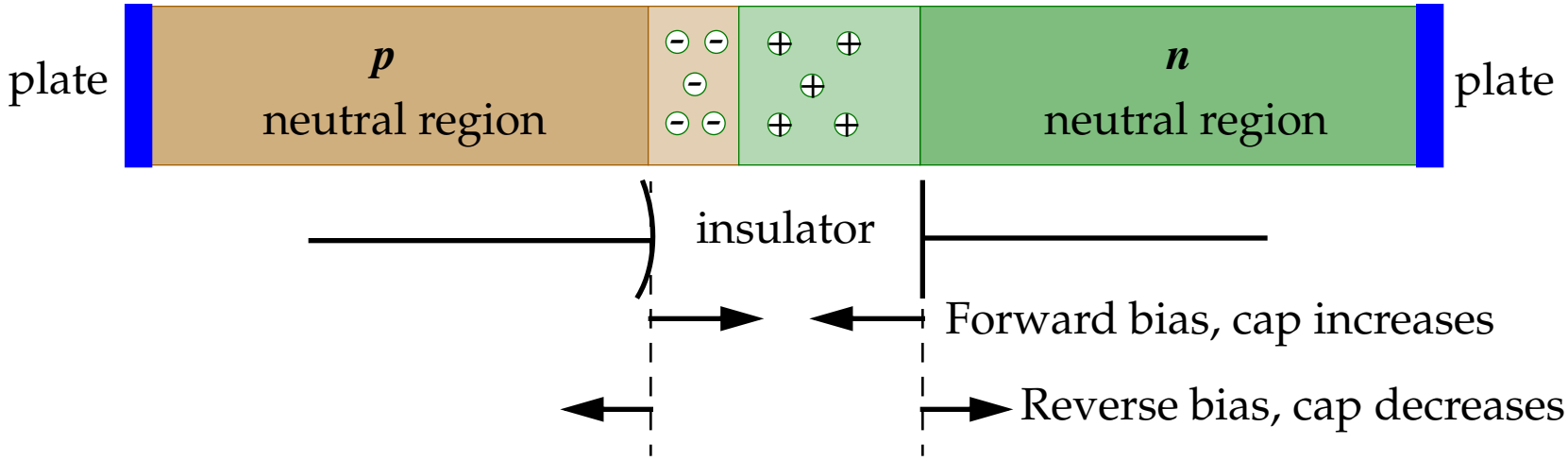
$$\frac{W_2}{(-W_1)} = \frac{N_A}{N_D}$$

Dynamic Behavior

The model (for an abrupt junction):

Imagine the depletion region as the **dielectric** of a capacitor with dielectric constant of silicon.

And the n- and p-neutral regions act as the capacitor plates:



A small change in the voltage applied to the junction (dV_D) causes a change in the space charge (dQ_j).

Dynamic Behavior

Depletion layer capacitance:

Junction capacitance is easily computed by taking the derivative of equation (1) with respect to V_D. For an abrupt junction:

$$C_j = \frac{dQ_j}{dV_D} = A_D\sqrt{\frac{\varepsilon_{si} q}{2}\frac{N_A N_D}{N_A + N_D}(\phi_0 - V_D)^{-1}} = \frac{C_{j0}}{\sqrt{1 - V_D/\phi_0}}$$

C_{j0} is the capacitance under *zero-bias* conditions and is only a function of the **physical parameters** of the device:

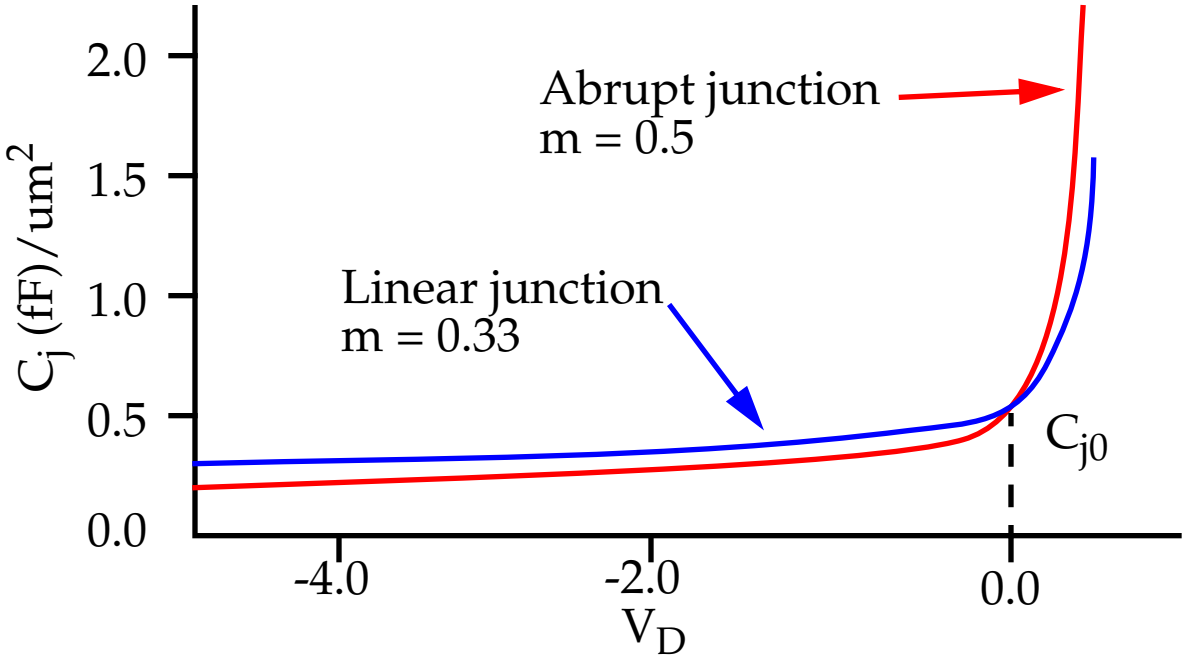
$$C_{j0} = A_D\sqrt{\frac{\varepsilon_{si} q}{2}\frac{N_A N_D}{N_A + N_D}(\phi_0^{-1})}$$

The same result can be obtained using the standard parallel-plate capacitor equation:

$$C_j = \varepsilon_{si}\left(\frac{A_D}{W_j}\right)$$ where W_j is given by equation (2).

Dynamic Behavior

Junction capacitance plotted as a function of applied voltage bias:



Strongly non-linear

Capacitance *decreases* with an *increasing* reverse bias.

For -5V, the cap. is reduced by more than a factor of 2 over the zero bias case.:

$C_{j0} = 2\times10^{-3}\,\mathrm{F}/m^2$

$A_D = 0.5um^2$

$\phi_0 = 0.64V$

then a reverse bias of -2.5V yields

$(0.9fF/um^2)(0.5um^2) = 0.45fF$

Dynamic Behavior

For the general case:

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

Where **m** is the grading coefficient.

- For an abrupt junction, m = 1/2.
- For a linearly graded junction, m = 1/3 (see previous figure).

For digital circuits, operating voltages tend to move rapidly over wide ranges.

In these cases, we can replace the voltage-dependent, nonlinear capacitance C_j with an **equivalent, linear capacitance** C_{eq}.

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{\text{high}}) - Q_j(V_{\text{low}})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)}[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Dynamic Behavior

For example:

Compute the average junction capacitance if this diode is switched between 0 and -5V.

$$C_{j0} = 0.5 fF/um^2$$
$$A_D = 12 um^2$$
$$\phi_0 = 0.64 V$$
$$m = 0.5$$

$$K_{eq} = \frac{-0.64^{0.5}}{(0-(-5V))(1-0.5)}[(0.64-0)^{1-0.5} - (0.64-(-5))^{1-0.5}] = 0.502$$

$$\text{Average} C_j = 0.502 \times 0.5 \text{fF}/um^2 = 0.25 \frac{\text{fF}}{um^2}$$

Secondary Effects

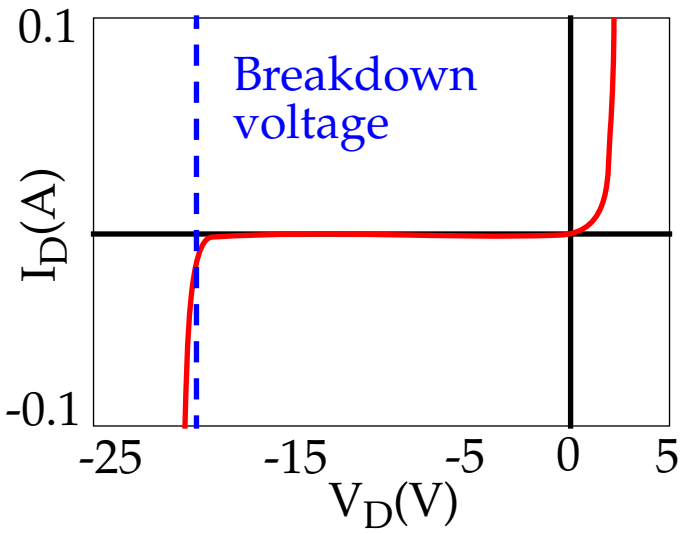
Actual diode current is less than what is predicted by the ideal eq.

Not all of the applied bias voltage falls across the junction, some falls across the neutral regions.

However, the resistivity of the neutral regions is generally small (1 to 100 Ohms).

This is usually modeled with a series resistance at the contacts.

Avalanche breakdown (MOS and bipolar processes):



Increased reverse bias increases electric field across the junction to E_{crit}.

Electron-hole pairs are created on collision with immobile silicon atoms.

Non-destructive but increases power consumption.

Secondary Effects

Operating temperature effects:

- The *thermal voltage* is linearly dependent upon temperature (increasing ϕ_T causes the current to drop).

$$\phi_T = \frac{kT}{q} \longrightarrow I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$

- The thermal equilibrium carrier concentrations **increase** with increasing temperature causing I_S to increase.

  Experimentally, the reverse current doubles every 8 degrees C.

These have a dramatic effect on the operation of the circuit.

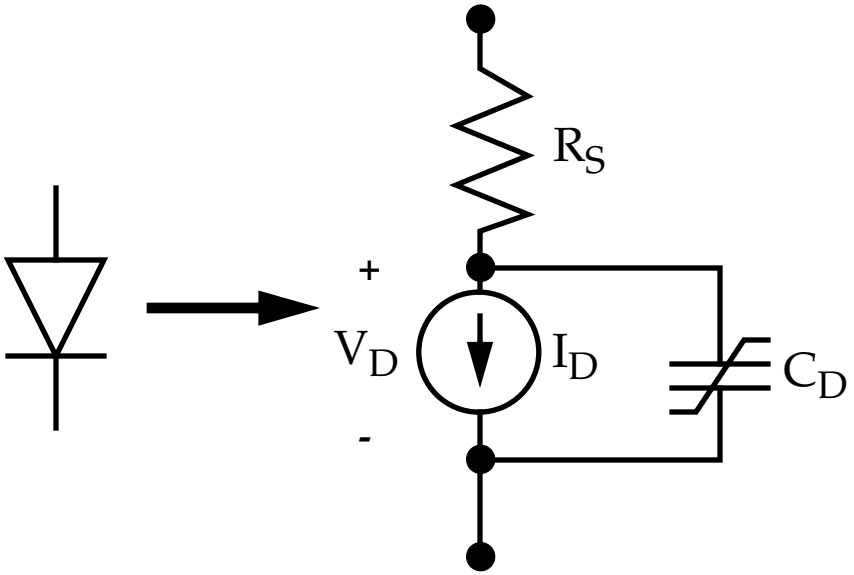
- Current levels can increase substantially (~2X every 12 degrees C).
- The increase in leakage current through reverse-biased diodes decreases isolation quality.

SPICE Models

The preceding discussion presented a model for manual analysis.

If second-order effects or more accuracy (better model) is desired, simulation is required.

The standard SPICE model:



$$I_D = I_S\left(e^{V_D/n\phi_T} - 1\right)$$

Extra parameter n is called the emission coefficient.

It is equal to 1 for most diodes.

R_S models the *series resistance* of the neutral regions (reducing current).

SPICE Models

The dynamic behavior is modeled by the *nonlinear* capacitance C_D.

Two different charge storage effects are combined in the diode:

- *excess minority carrier charge* (not discussed, forward bias only)
- *depletion-region charge*

$$C_D = \frac{\tau_T I_s}{\phi_T} e^{V_{D/n\phi_T}} + \frac{C_{j0}}{(1 - V_D/\phi_0)^m} \qquad \text{where: } \tau_T = \text{transit time}$$

Table 1: First-order SPICE diode model parameters

Parameter name	Symbol	SPICE Name	Units	Default Value
Saturation Current	I_S	IS	A	1.0E-14
Emission Coefficient	n	N	-	1
Series Resistance	R_S	RS	Ω	0
Transit Time	τ_T	TT	s	0
Zero-bias Junction Cap	C_{j0}	CJ0	F	0
Grading Coefficient	m	M	-	0.5
Junction Potential	ϕ_0	VJ	V	1