CMOS Processing Technology

Silicon: a semiconductor with resistance between that of conductor and an insulator.

Conductivity of silicon can be changed several orders of magnitude by introducing **impurity atoms** in silicon crystal lattice.

- Impurities that *use* electrons: acceptors (p-type), e.g., Boron.
- Impurities that *provide* electrons: donors (n-type), e.g., Phosphorous.

Wafer: 10 cm to 30 cm (~4" to ~12") and 1 mm thick.

Wafers are cut from ingots of single-crystal silicon, that have been pulled from a crucible melt of pure molten silicon at 1425 degrees C (*Czochralski* method).

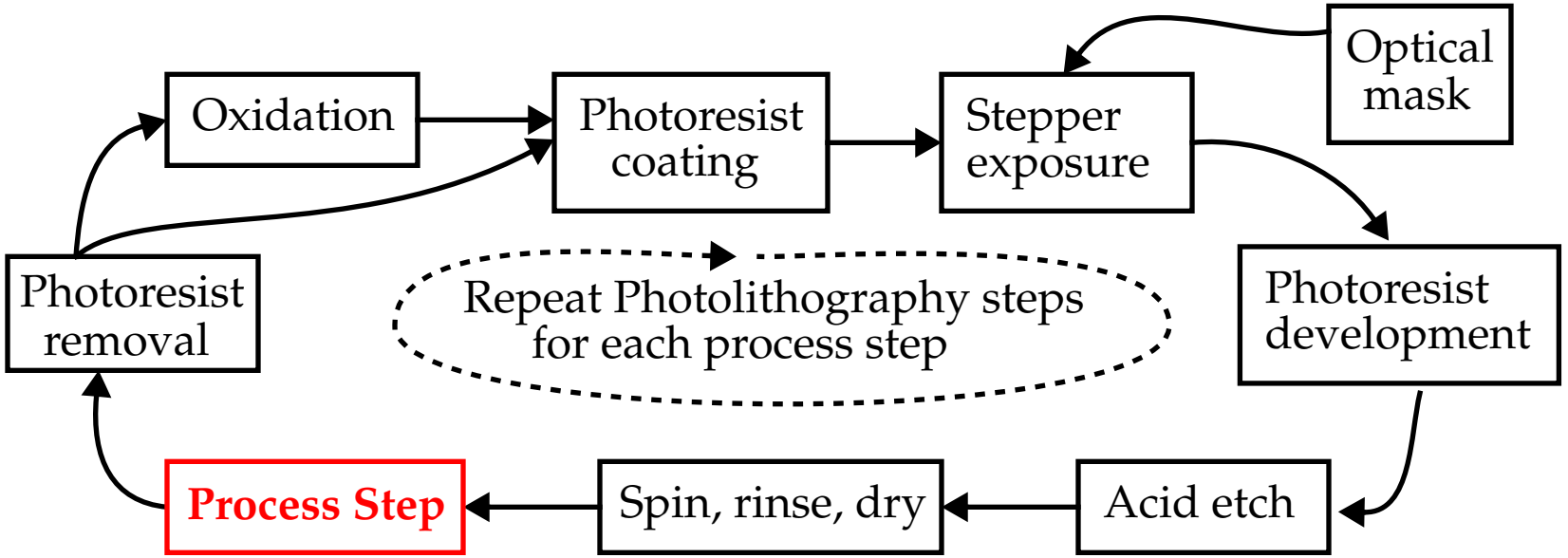
Controlled amounts of impurities are added to the melt to enable the proper electrical properties.

Photolithography

In each processing step, regions are selected for processing using photolithography and optical masks.

Processing steps include:

- Oxidation
- Etching
- Metal and polysilicon deposition
- Ion implantation



Photolithography Process

Oxidation layering

Creates a layer of SiO_2 or glass for insulation.

Wet Oxidation uses water vapor and **Dry Oxidation** uses high-purity oxygen and hydrogen at ~1000 degrees C.

SiO_2 growth consumes silicon, grows into the substrate.

SiO_2 is twice the volume of Si, projects above the substrate as well.

Photoresist coating

A light-sensitive polymer (latex) is evenly spread (thickness 1 μm) by spinning the wafer.

Negative photoresist: Unexposed photoresist soluble in organic solvent, light exposure causes cross-linking making exposed regions insoluble.

Positive photoresist: Originally insoluble, exposure makes it soluble.

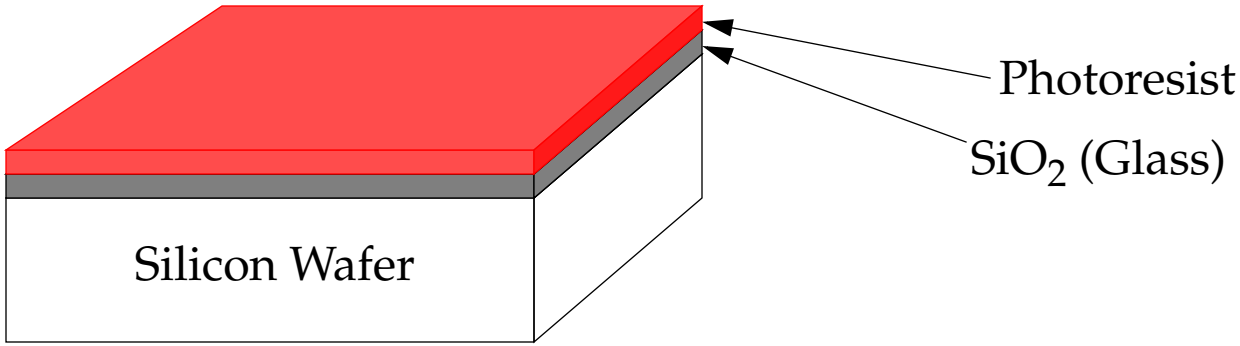
Combining allows a single mask to be used for processing of complementary regions in 2 processing steps.

Photolithography Process

Photoresist coating (continued)

For example, to cut windows into the glass after oxidation step:

Acid resistant coating (photoresist) spread evenly on surface.



Stepper exposure

A glass mask (**reticle**, about 2 cm per side) containing the designer patterns is brought in close proximity to wafer.

For *negative photoresist*, mask is opaque in regions to be processed.

Ultraviolet (UV) light exposes transparent regions making photoresist insoluble.

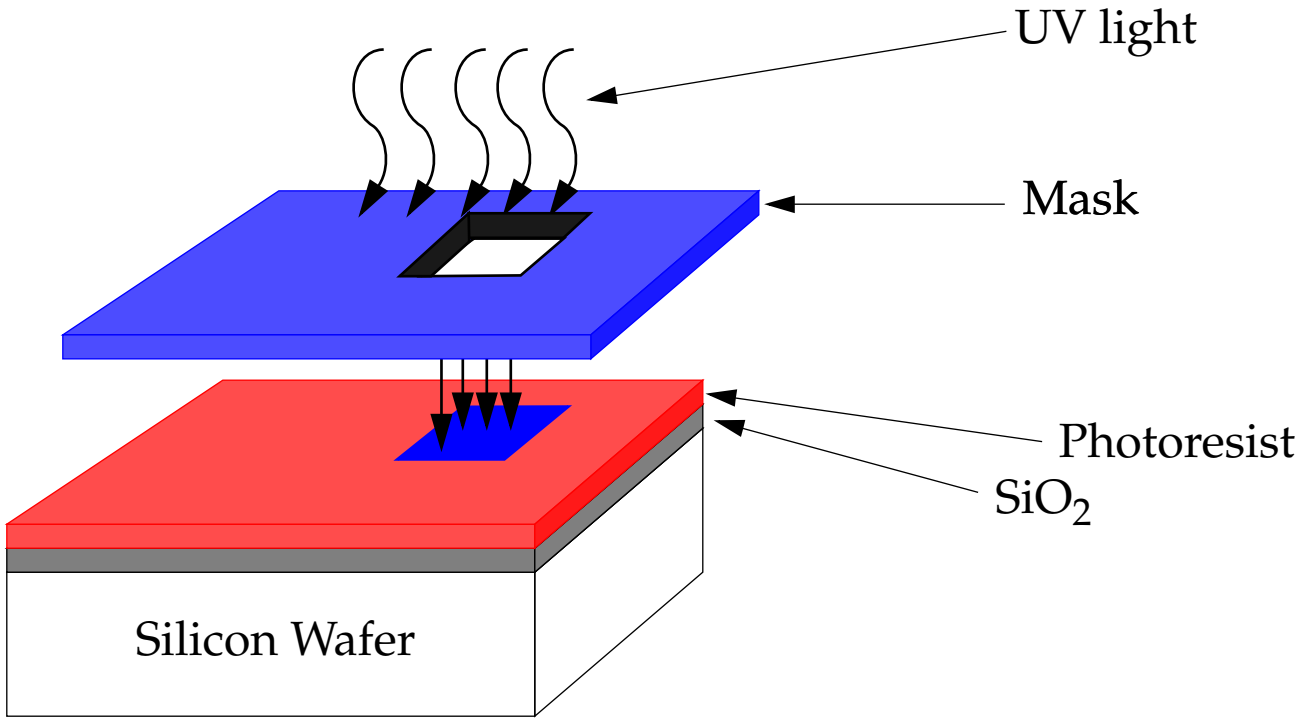
Photolithography Process

Stepper exposure (continued)

A *stepper* moves the reticle to successive locations on the wafer.

Projection printing makes use of lenses between reticle and wafer to focus the pattern.

Example: polymerized in areas exposed by UV light.



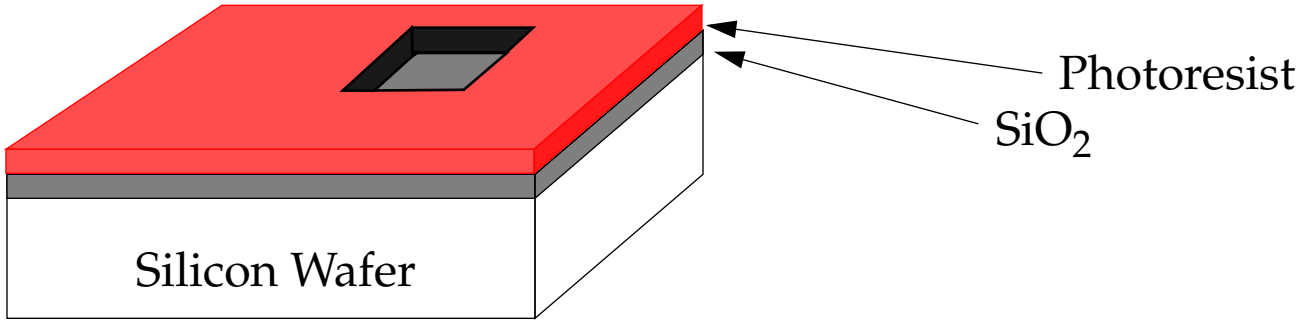
Photolithography Process

Photoresist development and bake

Wafers developed in acid or base solution to remove exposed/unexposed photoresist.

Once removed, wafer is low temperature *baked* (soft baked) to harden remaining (unexposed/exposed) photoresist.

Example: organic solvent removes polymerized areas.



Photolithography Process

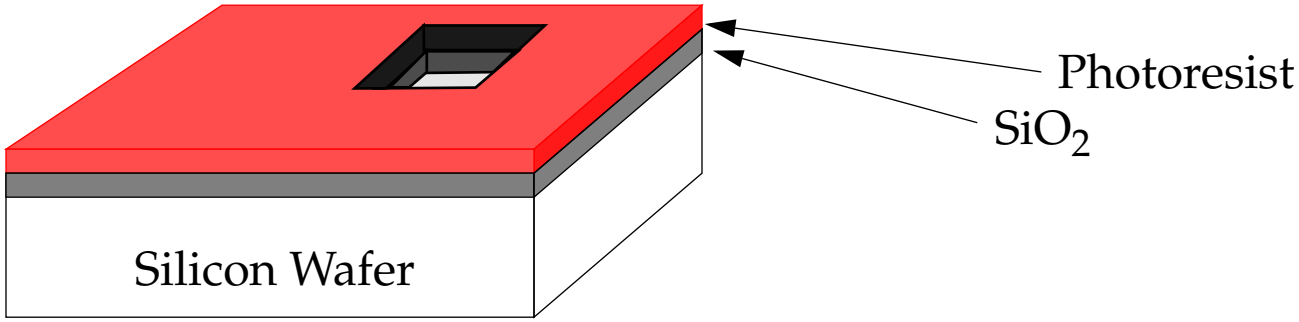
Acid etching

Material is selectively removed from areas that are not covered by photoresist using acids, bases and caustic solutions.

Chemicals used here can be very dangerous to humans and the environment.

Hydrofluoric acid (HF) is used for SiO_2.

Example: windows are etched using HF.



Photolithography Process

Spin, rinse and dry

The wafer is cleaned with deionized water and dried with nitrogen.

Cleaning reduces the chances of contamination.

All processing is carried out in ultra-clean rooms (dust particles per cubic foot of air are maintained at 1 to 10).

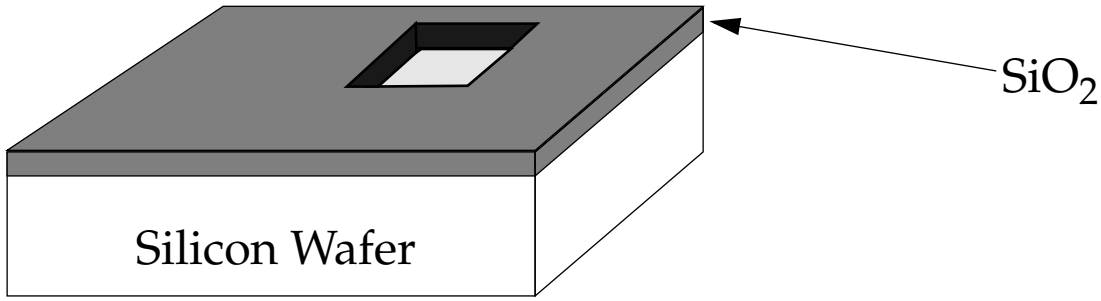
Processing step

A processing step can now be applied to the wafer, including ion implantation, plasma etching or metal deposition.

Photoresist removal (ashing)

A high temperature plasma is used to remove the remaining photoresist.

Example: photoresist removed.



Photolithography Process

Bear in mind that the example showed only one square that was etched.

In reality, the entire chip is patterned and etched in parallel, possibly creating *hundreds of millions* of such squares.

Feature size reduction puts an enormous burden on semiconductor equipment manufacturers, particular those involved with optolithographically.

The dimensions of features transcribed are smaller than the wavelengths of the optical light sources.

Optical mask correction (OPC) warps the mask's patterns to allow feature sizes down to ~100 nm to overcome the diffraction phenomena.

Phase shift masks (PSM) vary the thickness of the mask to create interference patterns.

These and other techniques increase resolution to 1/8 of the wavelength.

Sources are lasers at 248 nm and 193 nm (future 157 nm and 13.4 nm)

Extreme ultraviolet, X ray and electron beam are potential replacements.

Diffusion and Ion Implantation

Several steps in the manufacturing process require a change in the doping concentration of certain parts of the material.

- Source and drain regions
- Well and substrate contacts
- Doping of the polysilicon
- Adjustments to V_t

Several approaches exist, in the latter two, the regions to be doped are exposed and the rest of the wafer is coated with a buffer, typically SiO_2.

- **Epitaxy**:
  Single-crystal film grown on silicon surface with controlled impurities, that can have fewer defects than native wafer surface.

- **Diffusion implantation**:
  Wafers are placed in quartz tube and heated to 900-1100 degrees C.
  The dopants are introduced via a gas and diffuse into the surface following a guassian profile.

Diffusion and Ion Implantation

- **Ion implantation**:

  The system sweeps a beam of purified dopants ions across the surface. Acceleration determines their depth of penetration while exposure time determines their concentration.

Ion implantation more popular but requires a **thermal annealing** step to repair the silicon lattice.

Deposition:

Many of the layers of a CMOS process are introduced by deposition to act as either a buffer or as insulating or conducting layers.

SiO_2 was given earlier as an example.

Another is the use of silicon nitride, Si_3N_4, as a buffer for field oxide and stopper implant deposition.

Chemical vapor deposition (CVD) is used to deposit Si_3N_4 at temperatures of ~850 degrees C.

Deposition and Etching

Polysilicon is deposited using a CVD which flows **silane** gas (SiH_4) over a heated wafer coated with SiO_2 at ~650 degrees C.

Deposition is followed by an *implantation step* to reduce poly resistance.

Aluminum is deposited using **sputtering**, in which aluminum is evaporated using an electron-beam or ion-beam.

It is then etched to form the wire interconnect (subtractive process).

Copper is deposited selectively into trenches using a process called *dual damascene* (additive process).

Etching:

Wet etching already discussed as a means to remove (etch) SiO_2, typically hydrofluoric acid + ammonium fluoride.

Etching and Planarization

Dry or **plasma etching** is also popular.

Here, wafer is given a *negative charge* in a chamber heated to 100 degrees C under vacuum.

A *positively charged* plasma is introduced (usually a mix of nitrogen, chlorine and boron trichloride).

Rapidly moving plasma causes a chemical *sandblasting* action in the well defined direction of the electric field.

Clean vertical cuts can be etched using this method.

Planarization:

Chemical-Mechanical Planarization (CMP) is performed before each metal deposition layer to reduce the **step heights** in the SiO_2.

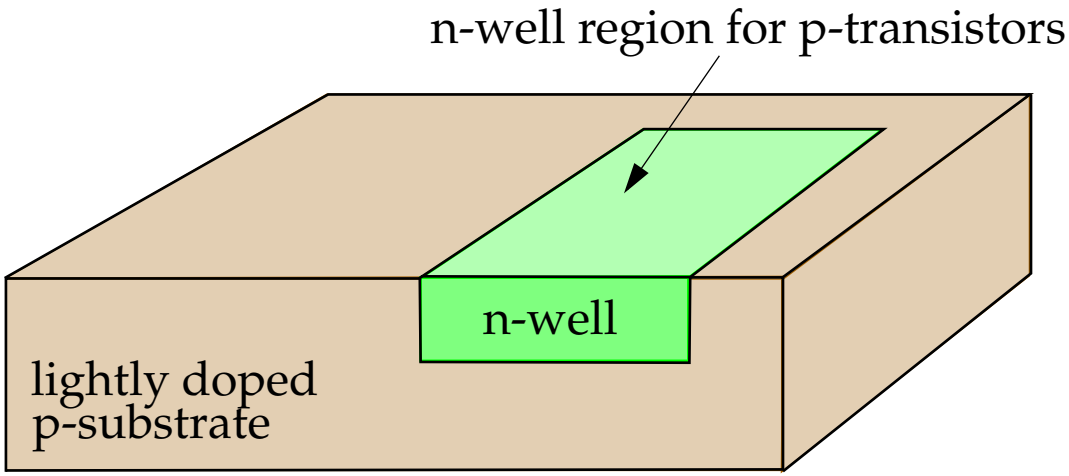
The process involves the use of a *slurry* compound, a liquid carrier with suspended abrasive components, e.g., aluminum oxide or silica.

CMOS Technologies

- n-well process
- p-well process
- twin-well process
- triple-well process
- silicon on insulator

Simplified CMOS process fl ow:

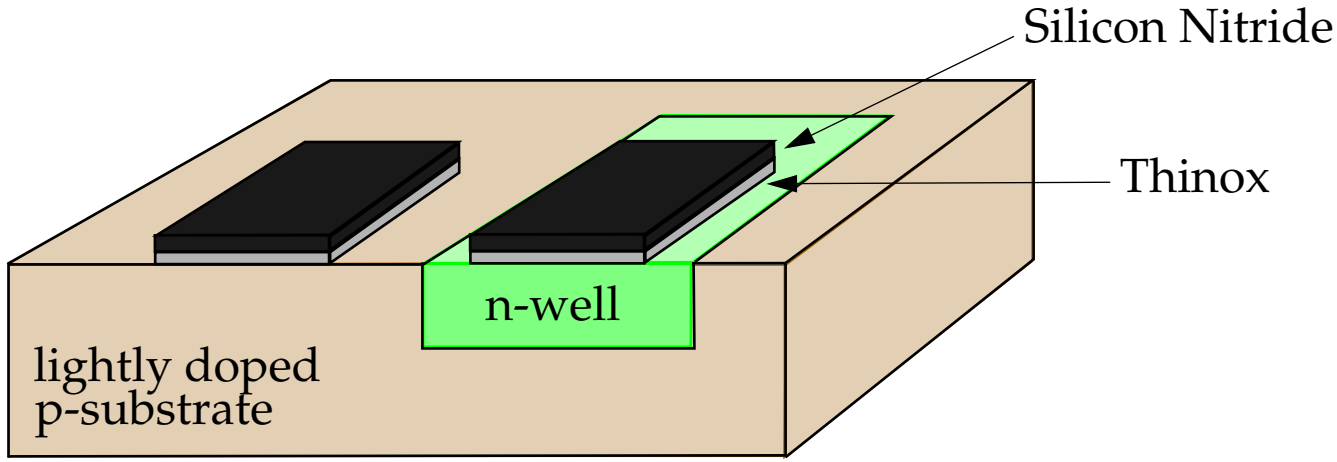
- *n-well mask* used to create n-well via ion-implantation.



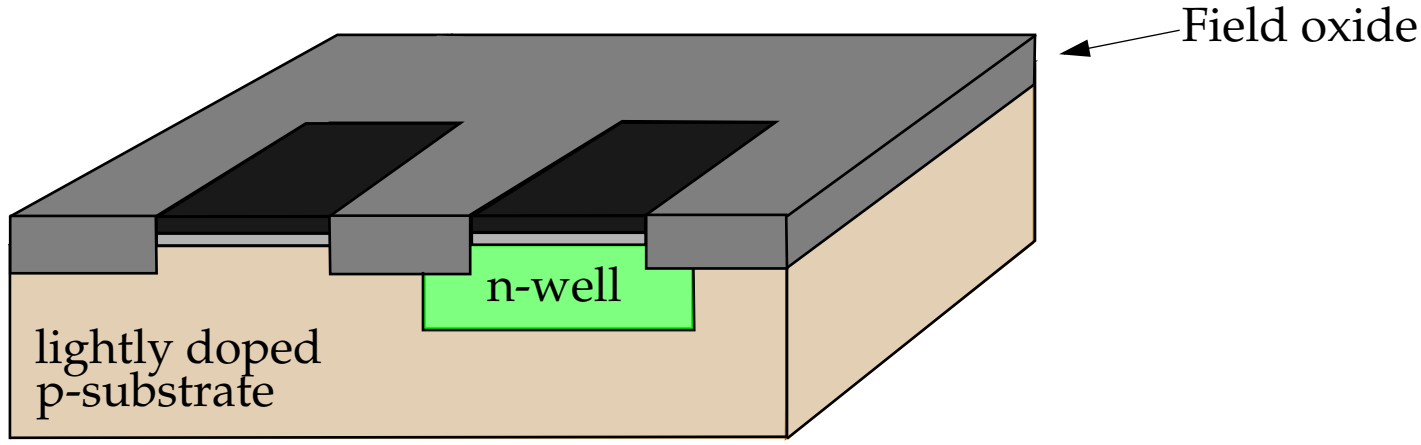
SiO_2 can be patterned as the mask for this step.

CMOS Processing Technology

- *active mask* defines areas where gates are fabricated.

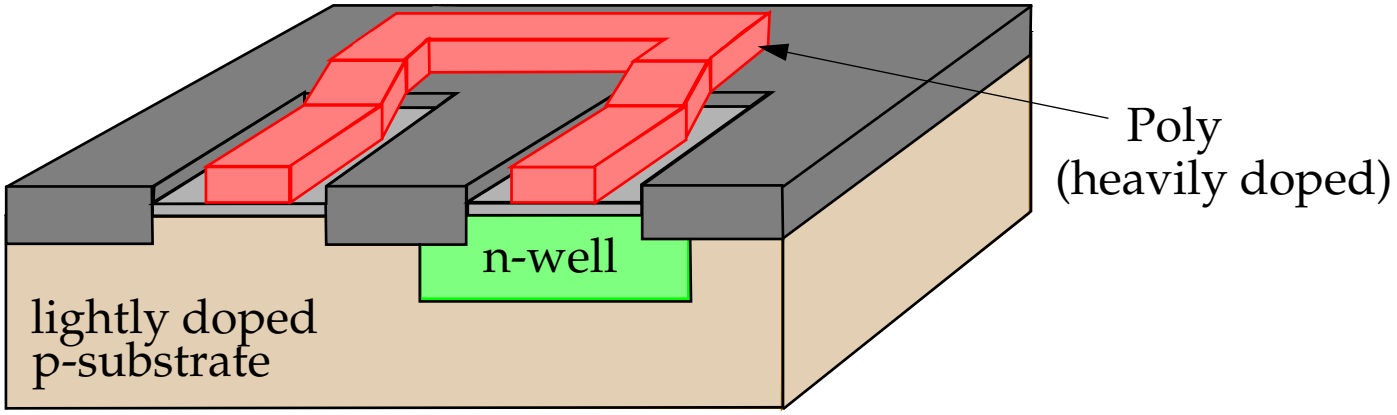


- Field oxide grown.

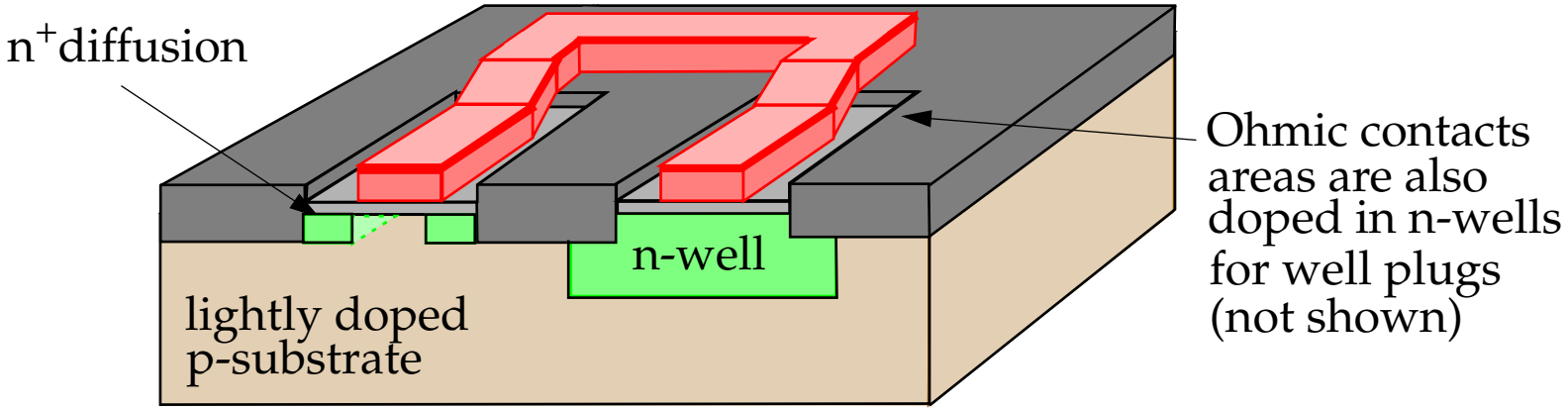


CMOS Processing Technology

- *poly mask* used to etch poly patterns.

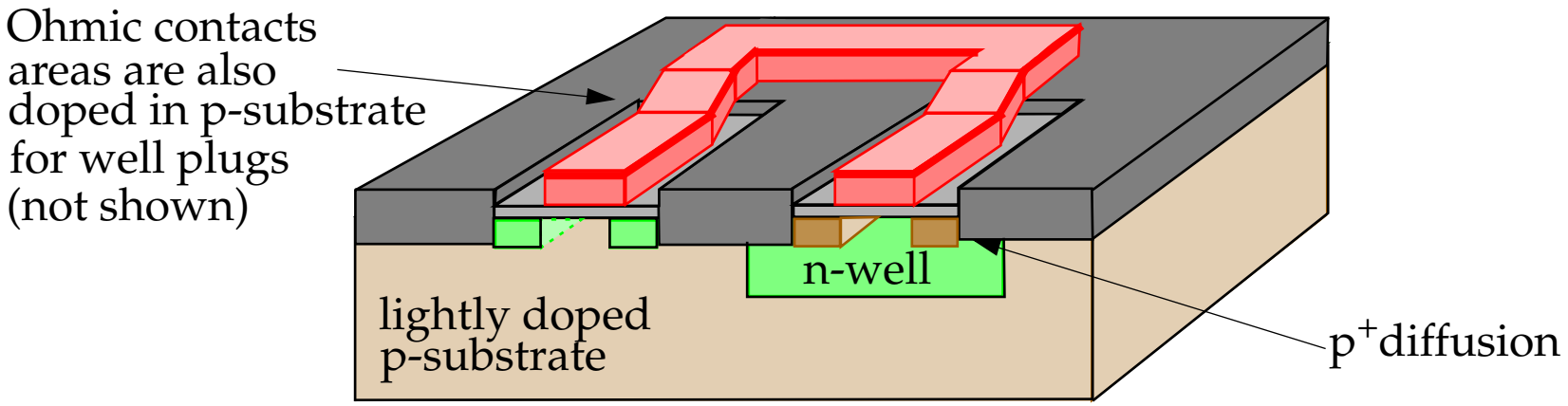


- *n-diffusion mask* used to select areas to implant n^+.

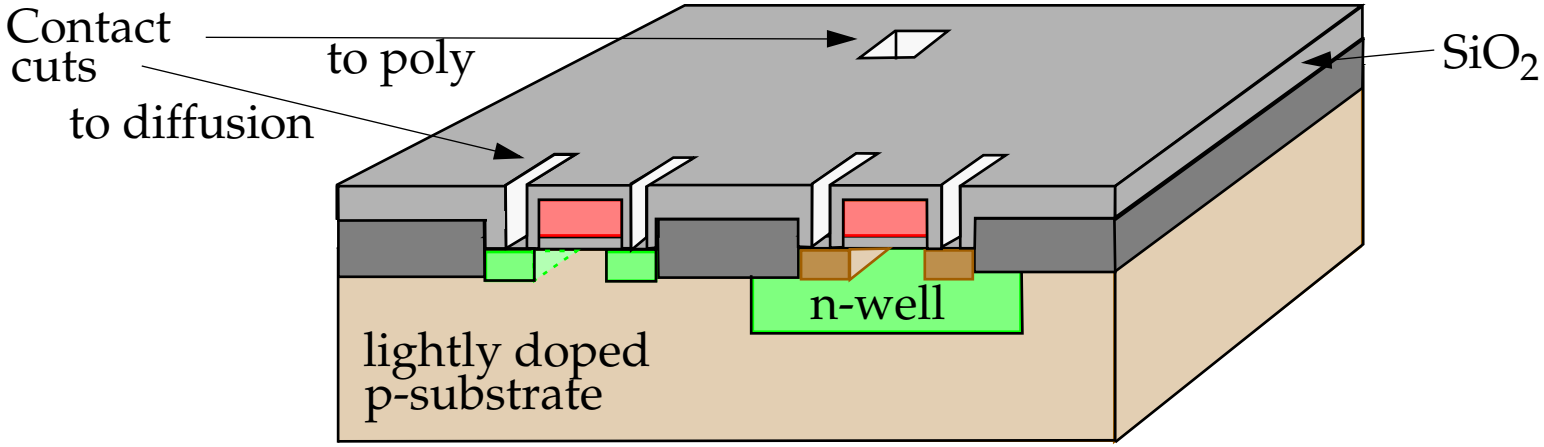


CMOS Processing Technology

- *p-diffusion mask* used to select areas to implant p^+.



- Surface is covered with SiO_2 and contact cuts made.



CMOS Processing Technology

- Metallization applied and etched using *metal mask*.