

Written Assignment #1 for CMPE 646

Assigned: Wed., Sept 19th

Due: Wed., Sept 26st, at the beginning of class

- 1) Distinguish between manufacturing test and design verification.
- 2) Explain what is portrayed by the Venn diagram on slide 6 of the introductory slides.
- 3) Explain the main purpose of testing, and the adverse impacts of yield loss and test escapes.
- 4) Explain why testing is getting more difficult as technology advances, i.e., what are the challenges?
- 5) Explain, as a function of time from first silicon to full blown production, the roles of go/no-go testing, diagnosis, burn-in, characterization test and failure analysis.
- 6) Distinguish between wafer probe testing and package testing, i.e., how are they different, what is or isn't possible, etc.
- 7) How is test data used, for what purposes?
- 8) Distinguish between functional testing and testing that uses functional vectors.
- 9) What is in-line testing?
- 10) Why is it difficult to do burn-in at wafer probe?
- 11) What are the costs associated with testing?
- 12) Explain the conflicting requirements of go/no-go testing.
- 13) Why is it difficult to obtain an exact value of yield?
- 14) Explain how the parameters, d and α , can be derived from negative binomial probability density function.
- 15) Adding DFT reduces yield and increases the cost of a chip. What purpose does it serve?
- 16) Why is defect level (DL) difficult to measure?
- 17) Explain how it can be estimated using test data.