Electrical and Computer Engineering Departmental Seminar:

Semiconductor Device Development and Modeling for Circuit Design and Simulation

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ABSTRACT
The semiconductor transistor dimensional scaling has contributed to improvement of transistor performance in the deep sub-micron processes for several years. Further dimensional scaling of the current CMOS devices in the nanometer range is using high-k dielectric material, metal gate and 3D FinFet architecture. The new scaling approach of using 3D architecture significantly decreases the device leakage power and short channel effects with each technology generation below 90-nm transistor channel length. However, the scaling of CMOS devices will eventually come to an end around 7-nm scale. At the end of this road map, transistor channel engineering using different materials with CMOS process is one of the alternatives to improve the device performance.

Speaker Bio Dr. Henok Abebe has been employed as Principal Member of Technical Staff (PMTS) by Sandia National Labs since 2012. He received a joint Ph.D. degree in Engineering and Industrial Applied Mathematics from Claremont Graduate University (member of the Claremont Colleges), California. He has more than 15 years of professional work experience in the semiconductor industry, academia, and US government national labs. His research interests include quantum mechanics, VLSI circuit simulation, and semiconductor device modeling.

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