Layout Tutorial

This tutorial will cover the basic steps involved in using the Cadence layout editor called Virtuoso. This document is supposed to be a general overview of the tool and more specifics can be found under openbook. To invoke openbook type '*openbook &*' at the command prompt. The paths and the necessary X windows environment setup should be completed before starting this tutorial.

The following steps will briefly summarize the steps involved in bring up ICFB which is the main cadence interface. All the commands should be executed without the quotes.

- First of all type '*xhost sunserver1.cs.umbc.edu*' in an xterm on the local machine.
- Next log on to sunserver using telnet or ssh.
- Setup the display by typing '*setenv DISPLAY* local_machine*:0*' where local_machine stands for the name of the local machine on which you are working.
- Invoke icfb from the proper directory (generally ~/cadence/cell_design/) by typing '*icfb &*' at the command prompt.

This will bring up the main icfb interface (Figure 1) and the library manager (Figure 2) windows. Sometime a third window named What's new in 4.4.3 pops up. It is just a text readme file which you can close.

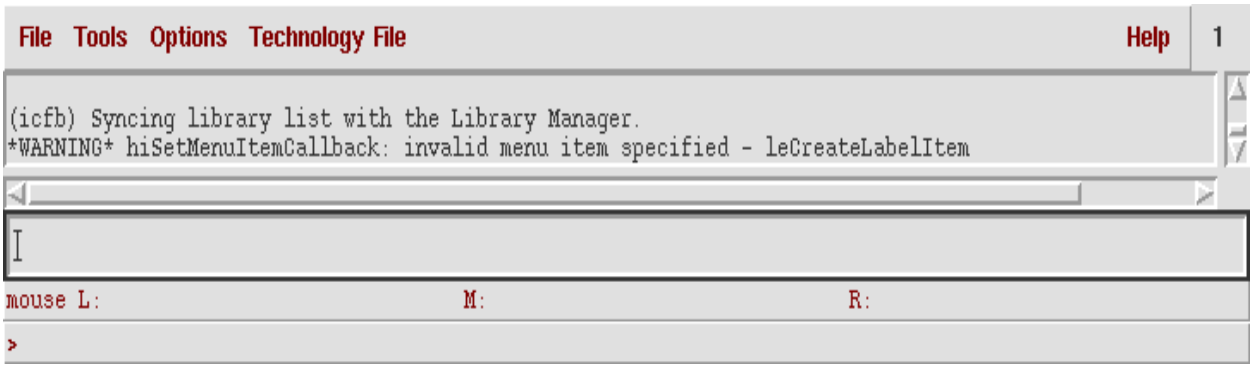

Figure 1. ICFB main window.

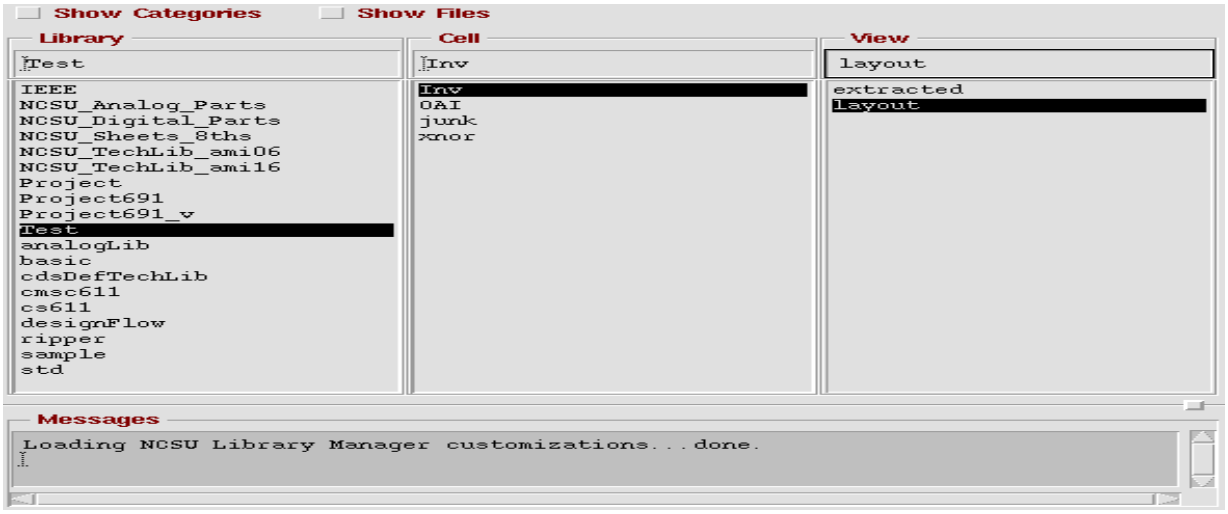

Figure 2. Library manager window.

The main icfb window is used to open the tools available in the cadence distribution. The library manager window is a browser which lists all the default design libraries defined in your cds.lib file as well as the custom libraries that you make. To start a design you first need to make a library. The library should have a technology file attached to it that defines all the layout rules you can use for that particular feature size. The library menu can be accessed by clicking File - New - Library in the main icfb window. The library dialogue box is shown in Figure 3.

Figure 3. New library dialog box.

To create a new library specify the name of the library in the *Name* box in the above figure. Click on the *Attach to existing tech library* option and attach a technology file that you are supposed to use. The technology file defines the minimum feature size that you can use. The λ value for the library is defined as half the feature size. Click *OK* in the above form and a new library by the name that you specified will show up in the library manager window under the library column. Now to draw the layout for a design you need to create a cell view in the library that you just created. Choose File - New - Cell view in the library manager window. The create new cell view dialogue box pops up as shown in Figure 4.

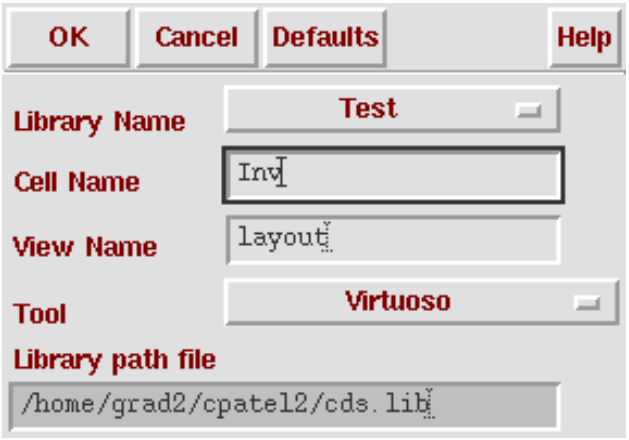

Figure 4. Create new cell view dialogue box.

Select the library that you want to make the new cell view in the library selection menu. Next give a name to the cell view in the *Cell name* box. To create a layout view select the *Virtuoso* tool in the tool selection menu. The *layout* view will automatically appear in the *View name* box. The example that we are going to use in this layout is a full complementary inverter. The library name is *Test* and the cell view is called *Inv.* Click *OK* and the new cell view will be displayed in the

library manager window under the cell view column for the library selected in the library column. Also the view that you are using will be displayed in the view column. There are different views that you can create for the same cell. Along with updating the library manager window two windows will pop up when you create the new cell view. A layout window and an LSW window. The layout window is the main window where you do your design layout. The LSW or the layer selection window gives you a list of all available layers in the current technology. They will include layers like poly, nactive, pactive, nselect, pselect, metal1, cc, via etc. depending on the technology you are fabricating in.

To start the layout the first thing that you need to do is fix you grid sizing. It is usually done by default but you can check it using the Options - Display dialogue in the layout window. The options window shown in Figure 5 will pop up.

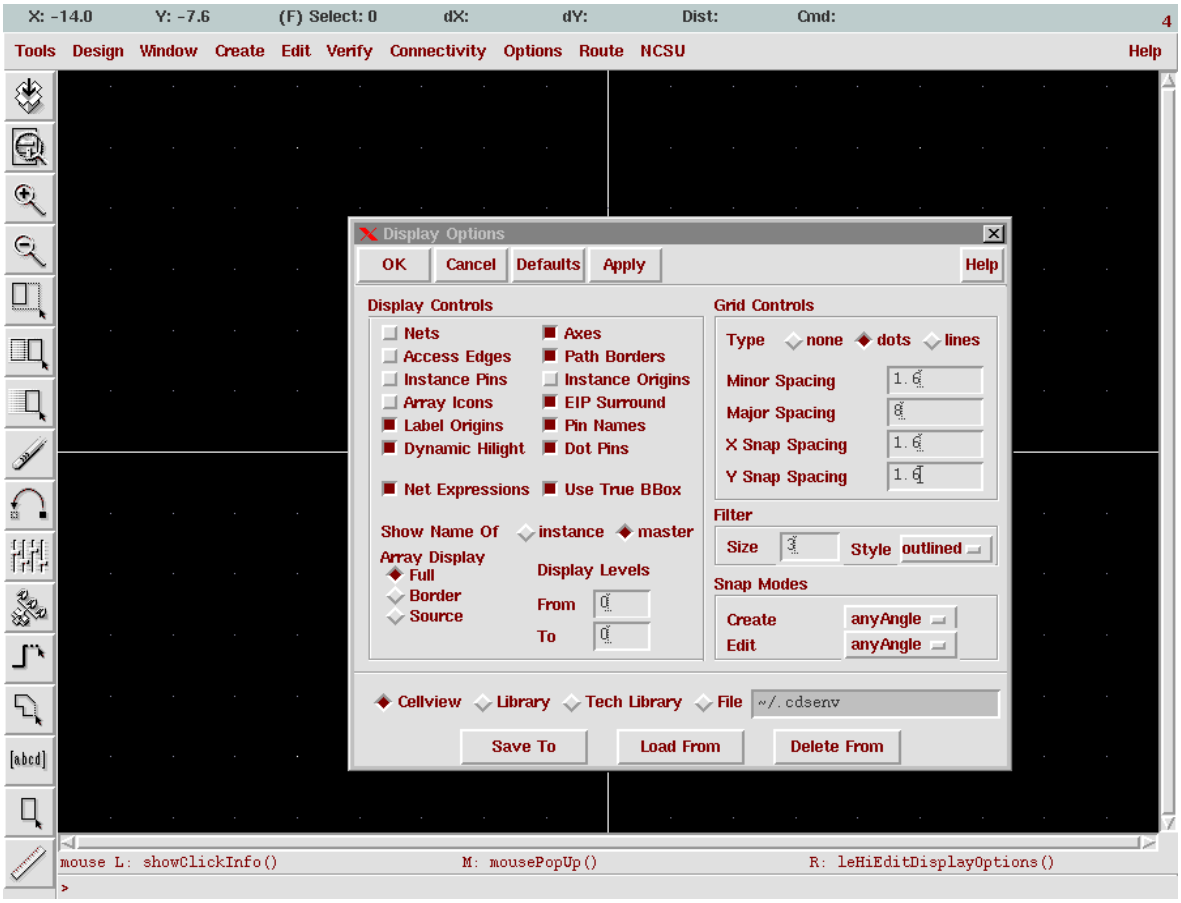

Figure 5. Display options dialogue box.

Check the grid control parameters in the right hand upper corner have the following values.
Minor Spacing = 2λ
Major Spacing = 5λ
X Snap Spacing = λ
Y Snap Spacing = λ.

Remember λ is half the feature size so if you are using a 1.6 υm. process then the λ value is 0.8. Also make sure that the *Snap Modes Create and Edit* settings in the right bottom corner are

set to *anyAngle.* Click *OK* and then go the Window option on the main screen and click *redraw.* This will set up the grid spacing according to requirements of the technology.

A brief description of how to actually create a inverter layout is described below. To learn the different menus in the layout window please refer to openbook documentation. To make an inverter first of all you need to make p and n transistors. First we will make the p transistor. Most of the technologies you will be designing in will use a n-well process. Therefore the black background in the main layout window will act as your p-substrate. Thus you can put n transistors directly in the p substrate. However your p transistor will have to be placed in n-well that you will have to draw specifically. Figure 6 shows the different layers required to built a p transistor.

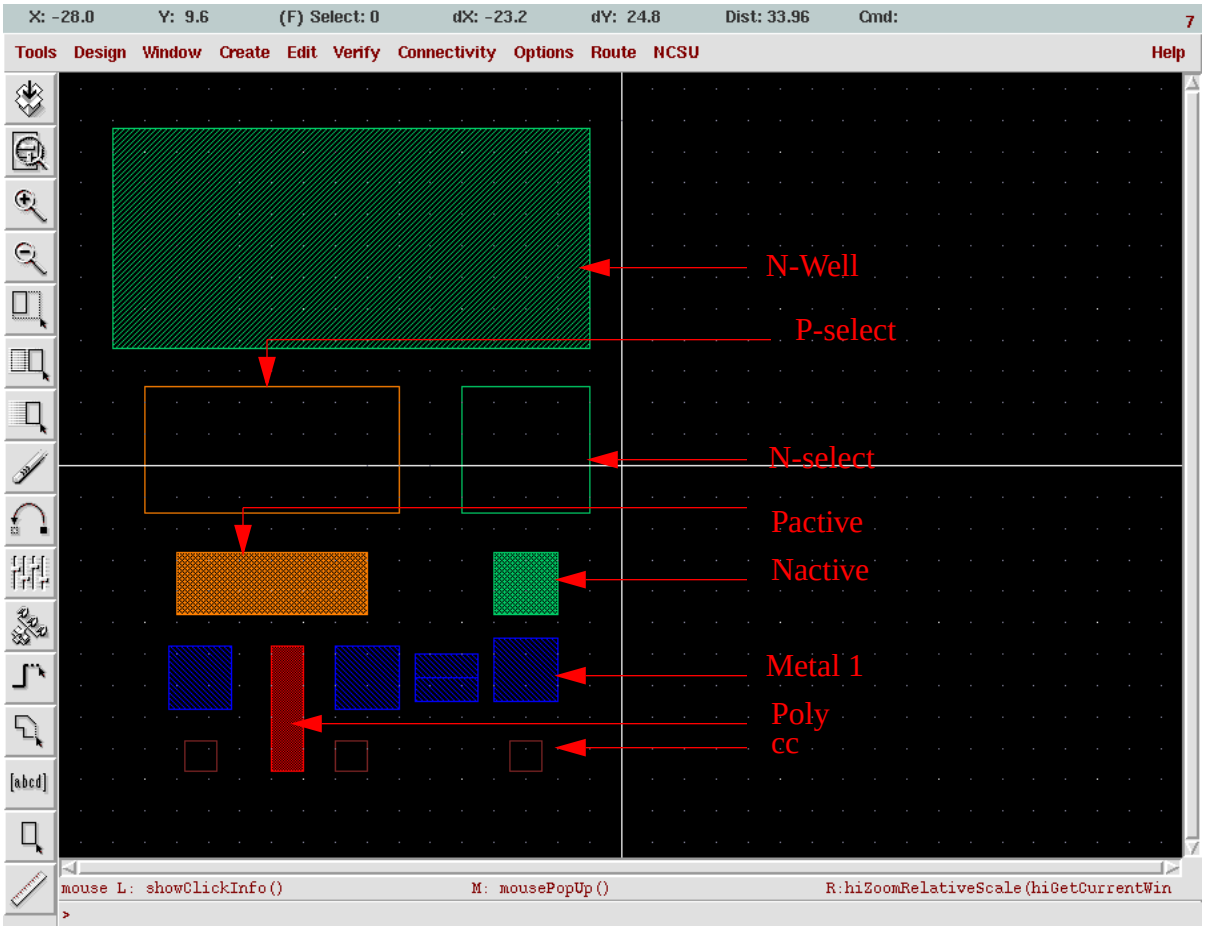

Figure 6. Layers required to built a p transistor.

The p transistor is made by using the layers as shown in the figure above. The size of the layers depend on the DRC rules defined for the library and they can be accessed at the following website:- *www.mosis.org.* Go to technical support and then to mosis design rules and select the technology that you are using. There is a rule checking tool that is available with the cadence distribution which checks most of the rules. The description of the tool is included at the end of this tutorial however you need to run the design rule checker at every step of you design. It is very difficult to fix up the sizes of various components after they are connected together in the layout so make sure that everything that you place in the layout is compatible with the design rules. The p transistor is placed in the nwell and a n contact is placed in the nwell to connect it to Vdd. The

layers needed to make the p transistor are cc, metal1, pactive, poly and pselect. The pselect region should cover the entire active area and the poly gate. The nwell should surround the entire ptransistor along with the select region. Now you need an ncontact to connect the nwell to Vdd. The nwell is made up of cc, nactive and metal1 surrounded by a nactive rectangle. The contact is placed inside the nwell and then connected to the main Vdd supply rail in the design. The layers shown in the figure above are merged together as shown in Figure 7 to form the entire p transistor. The order in which the layers are placed is not important the only requirement is that all the layers should be present. The layers are displayed in the layout window as defined by the tool and the overlap of two different layers will be clearly distinguishable.

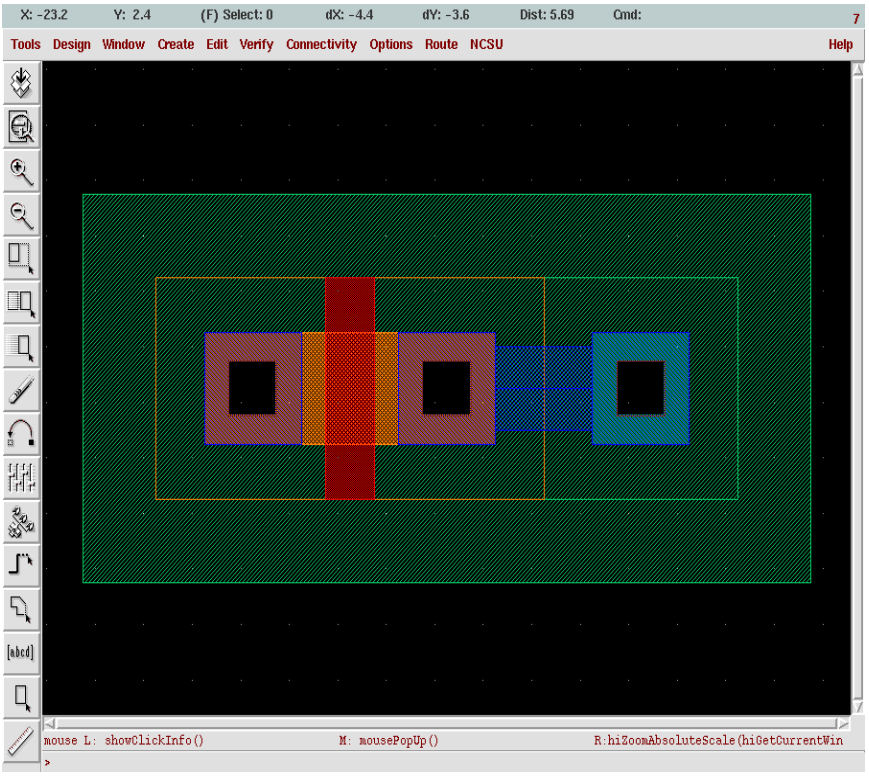

Figure 7. p transistor layout.

The n transistor is layed out in a similar fashion and the layers required for the same are shown in Figure 8. However the n transistor will have an nactive layer instead of pactive layer in the p transistor and will be surrounded by n select instead of the p select. As the technology is a nwell technology the black background is the p-substrate and therefore you need not put a pwell layer around the n transistor. However you still need to place a contact to connect the p substrate to Vss or ground. The p contact is complementary to the n contact and is made of cc, pactive and metal1 surrounded by a pselect rectangle. The combined p and n transistor are shown in Figure 9. The next step to build the inverter is to connect the drains of the two transistors together to make up the output. The source of the p transistor is connected to Vdd and the source of the n transistor is connected to Vss. The two gates are connected together to form the input of the inverter. The icfb Path command is the easiest way to connect components together in a layout. There are rules that define the minimum spacing required between two metal1 paths and so on which are listed on the mosis site. Figure 10 shows the entire layout for the inverter.

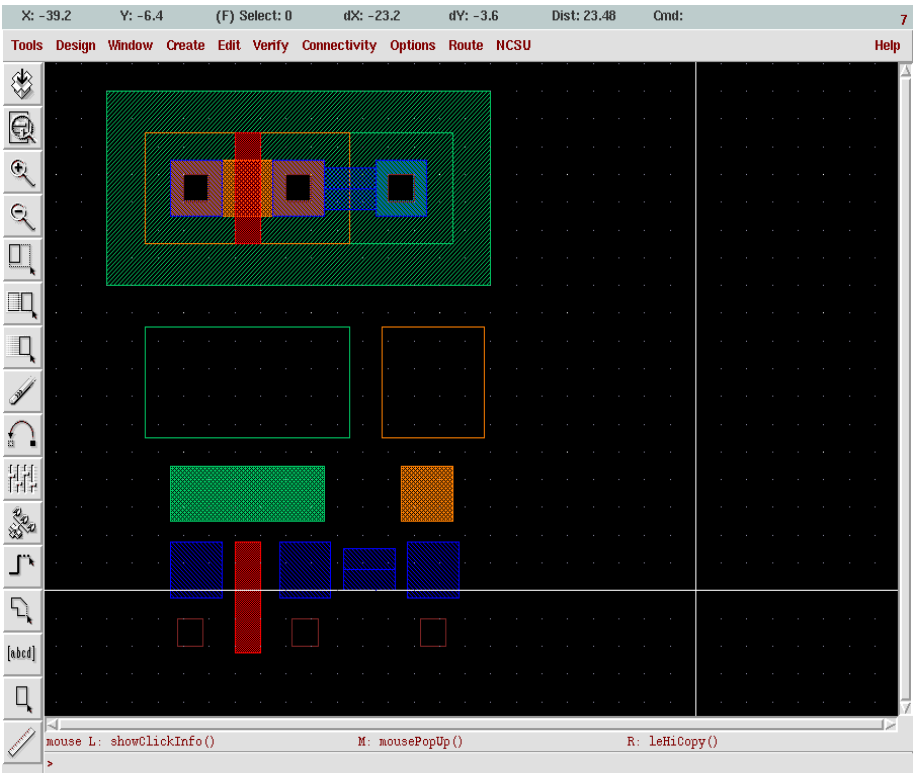

Figure 8. Layers required for the n transistor

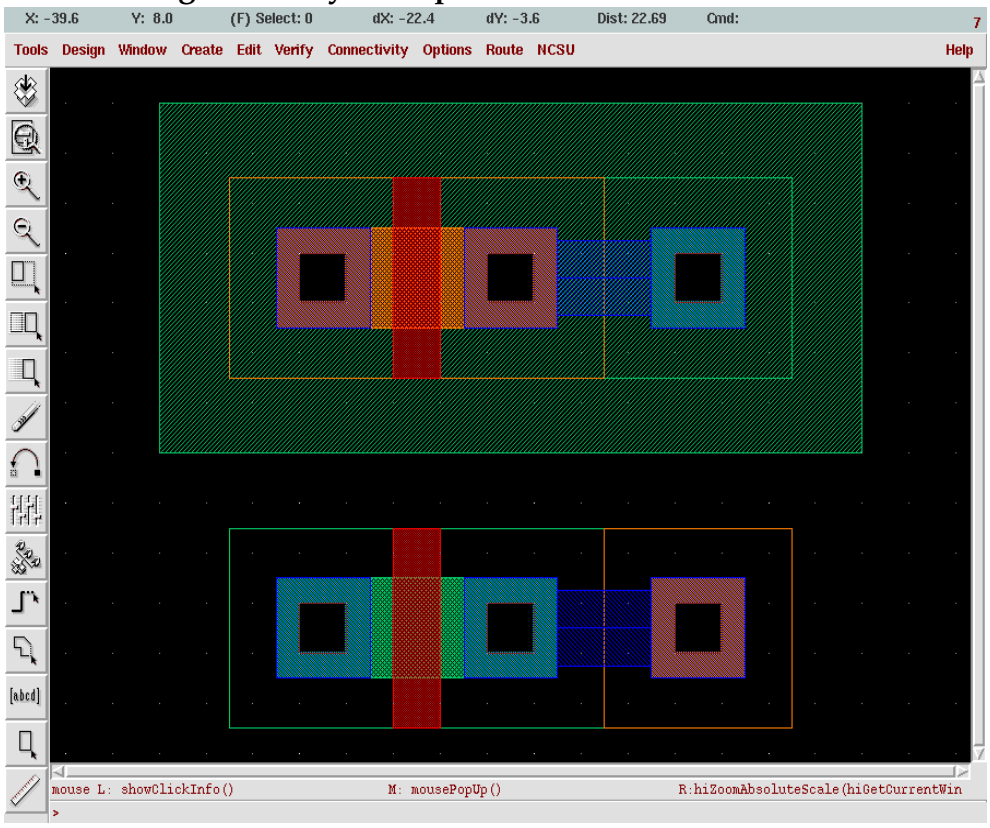

Figure 9. n and p transistor layouts.

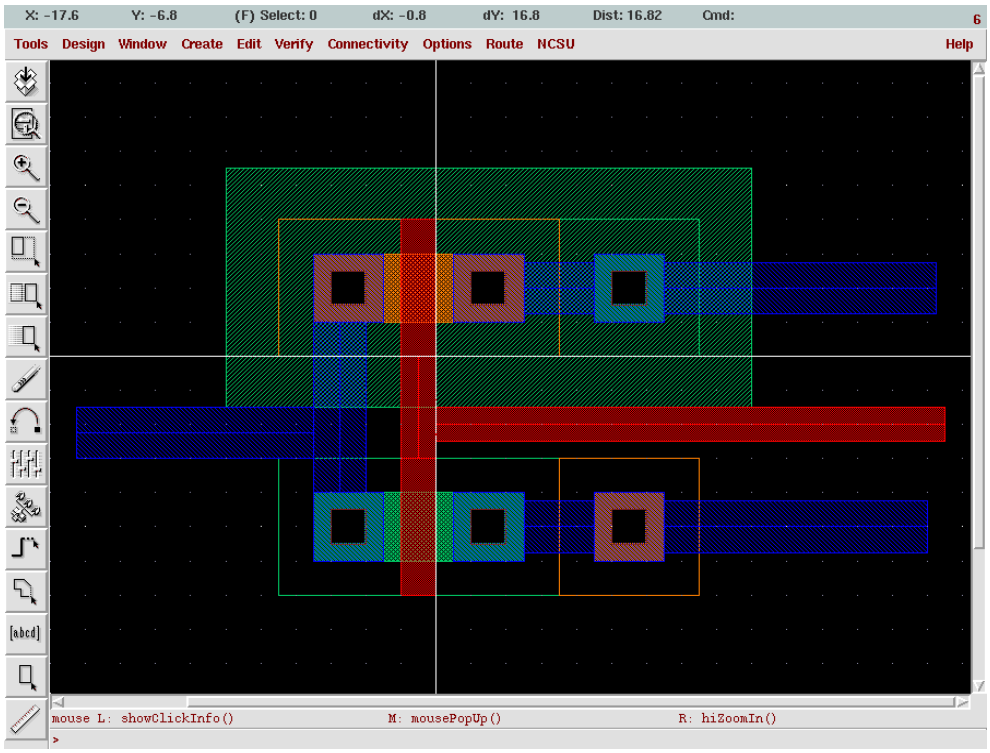

Figure 10. The entire inverter layout.

To complete your layout you need to place input or output pins at the various inputs and outputs of you circuit. This is done using the Create - Pin dialogue box shown in Figure 11.

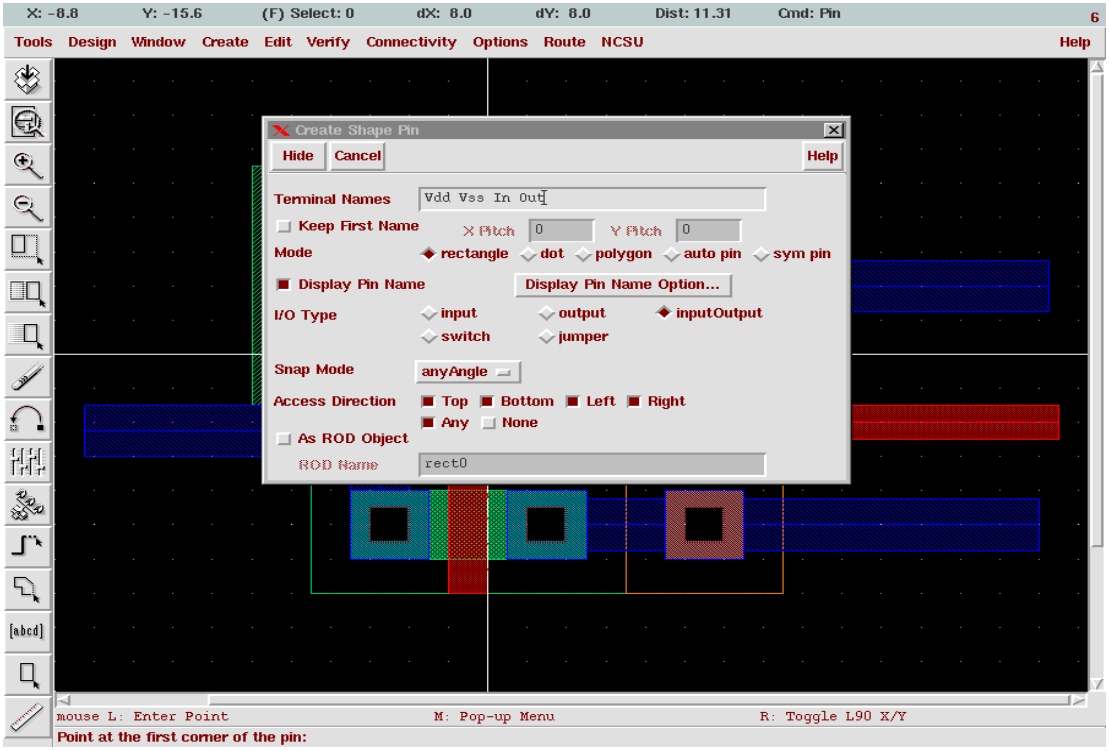

Figure 11. Create pin dialogue box.

In the *Terminal Names* box enter the name of the pins that you want to place in a space separated format (e.g. *Vdd Vss In Out* for the inverter). Please do not use a pin called gnd! or vdd! in your layout because they are the default pins used by the tool. Then click on *shape pin* in the *Mode* selection men. Next click on *Display Pin Name* button to turn the option on. Next select the *I/O type* for the pin. This will have to be changed individually for each pin. Thus the pin In in the inverter will have an I/O type of input whereas the pin Out will have I/O type as output. Next click on *any* in the *Access Direction* selection menu. To place the pins now select the proper layer from the LSW. Thus in case of the inverter the input pin has to be placed in the poly gates therefore select poly in the LSW. Now draw a small poly rectangle on the path connecting the two gates. The name associated with the pin will be displayed and click anywhere near the pin to put the name along side the pin. Now go to the pin menu and select I/O type as output for pin out. Select metal1 from the LSW because the output is the metal1 path connecting the two drains. Create a small rectangle of metal1 on the path and place the pin name beside it. Remember that you have to place the pins in the layout in the order that you specified them in the Terminal names list in the pin dialogue box. Thus for this example first place Vdd then Vss then In and at last the out pin. Also remember to change the I/O type for each pin and the layer that they are to be placed in.

As mentioned before all the layers have fixed sizes defined by the design rules. Also the separation between different layers is defined by the design rules. To check that your design is compatible with the design rules you can use the internal design rule checker tool called DRC. To invoke DRC go to verify and click DRC. The DRC dialogue box will pop up as shown in Figure 12. Click OK on the form and the rule checker will report all the error in the main icfb window in a text format. Also all the design rule errors will be marked using markers in your layout window.

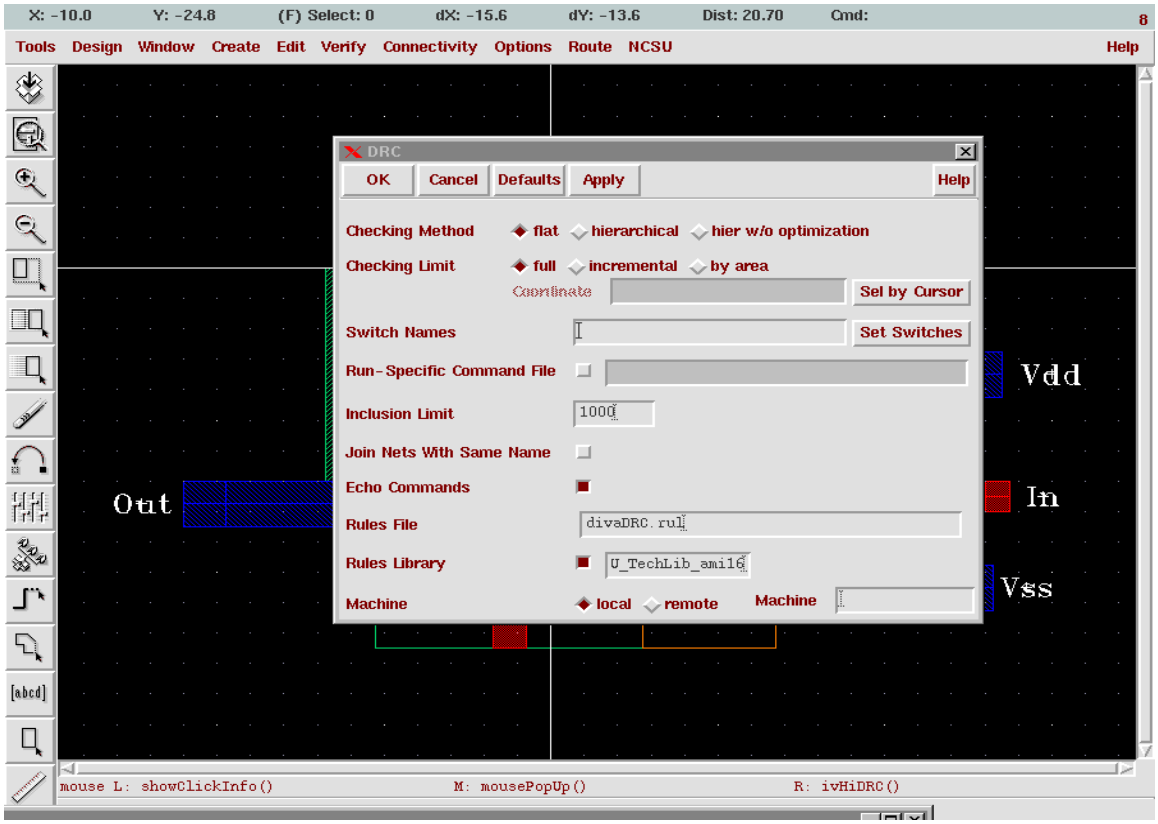

Figure 12. DRC dialogue box.

To check which marker stands for which error click on Verify - Markers - Explain and then click on any marker in the layout window. A text box will pop up specifying the design rule that is being violated. Fix the error in your layout and run DRC until your design is completely error free.

The following section will provide general help on some of the frequently used menu items.

Design Menu:

- *Save*:- save you layouts.
- *Properties*:- Select any layer in the layout and click properties to get specific information about that layer. You can change the layer definitions by changing their properties in the edit menu and the changes will be reflected in the layout window.
- *Plot*:- Used to generate a postscript file for your layout for printing. Select submit and then plot options. Specify a file name and click ok. Then click ok on the main submit plot form and it will generate a ps file for you layout.

Create Menu:

- *Rectangle*:- creates a rectangle of the layer selected in the LSW.
- *Path*:- Creates a path of the layer selected in the LSW. Double click to end the path.
- *Instance*:- used to import another existing cell view into this cell view.
- *Pin*:- Create pins as explained above.

Edit Menu:

- *Undo*:- undo the previous commands.
- *Redo*:- redo undone commands.
- *Move*:- click on any object and move it around in the layout.
- *Copy*: - Create a copy of any object in the layout.
- *Stretch*:- Click on the edge of a rectangle and size it.
- *Delete*: - Delete an object in the layout.
- *Properties*:- Change the properties of objects in the layout. Change the layer definitions and the changes are immediately reflected in the layout.

Verify Menu:

- *DRC*:- Check the layout for design rule violations.
- *Extract*: - Create a extracted view of the layout. This view is used for simulations.
- *Markers*:- *Explain*: click on the marker to find out the design rule violated.
  Delete all: Remove the markers after a DRC run.

More detailed description of each of the menu items can be found in the openbook documentation under the virtuoso layout editor.

The next section will cover some of the common DRC errors and their interpretations.

(SCMOS Rule 3.1) poly width: 1.60 um.

The poly width is less than the minimum required 1.6 um for this particular technology. Errors for width for any layer of the layout will have a similar format.

(SCMOS Rule 7.2.a) metal1 spacing: 2.40 um

The minimum separation requirement for metal spacing violated. All spacing errors will have a similar format.

(DBM Rule 2.0) Poly cannot overlap ohmic diffusion.

The p transistor is not placed in an nwell.

(DBM Rule 1.1) Active must be inside select.

The active layer was not surrounded by a select layer.

Most of the errors found by the design rule checker are explained in detail in the icfb window and are easy to fix. Sometimes a layout may not have DRC errors but only warnings. It is better to solve these warnings before going further. The most common warning is for pins. When you place two pins on the same path the DRC tool will generate a warning marker but will not explain it in the icfb main window. Use the verify - markers -explain menu in the main layout window to find out the warning description.