CMPE 413/CMSC 711 Exam I

Name:

This exam is 8 pages long and has 4 questions.

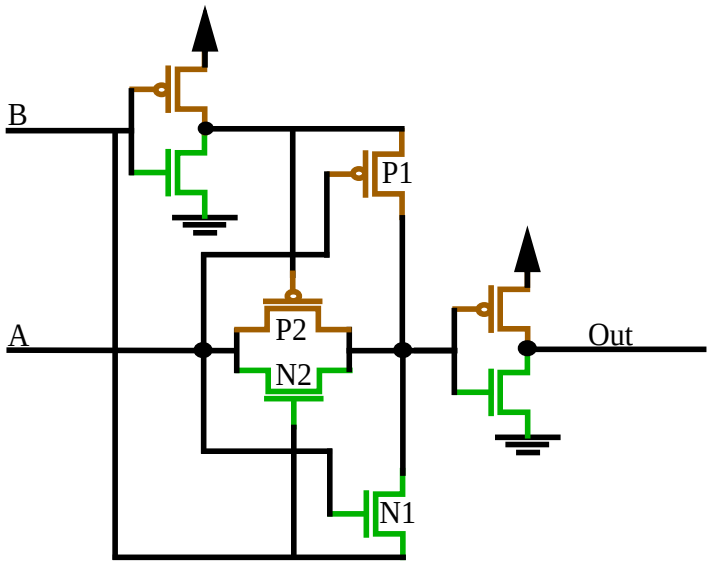
You must show all of your work -- partial credit may be given to partially correct answers, while answers with no justification may not receive full points. Use the back of the exam sheets if you need extra space.

1) a) (6pts) Define hierarchy and abstraction in the context of digital design. List three (of five) levels of abstraction in digital design. Briefly explain how hierarchy and abstraction are used to deal with design complexity.

b) (6pts) Design automation does not solve all of the problems associated with designing a digital integrated circuit. Briefly describe three reasons (of the seven discussed) that justify the importance of understanding digital circuit design.

c) (8 pts) Draw and label the **terminals** and **substrate doping** of an nMOS and a pMOS transistor cross-section forming a CMOS inverter, including the well(s). Briefly explain the biasing conditions of the source, drain and well(s) when 0V is applied to the input.

2) a) (6 pts) Give the truth table for the following transistor level schematic. Explain the source of 'good' logic 0's and 1's (using the labels P1, P2, N1 and N2) under each of the four input combinations.



b)(6 pts) Give the minimum CMOS realization of an XNOR ($f = \overline{a \oplus b} = ab + \bar{a}\bar{b}$). Assume the **un**complemented inputs ***a*** and ***b*** are available. Show your work.

b) (8pts) Give the minimum CMOS realization of the carry-generate function $c_{out} = c_{in}(a+b)+ab$. Assume the **un**complemented inputs $\boldsymbol{a}$, $\boldsymbol{b}$ and $\boldsymbol{c_{in}}$ are available. Is an implementation possible in which the p-tree is symmetric (not the dual) of the n-tree?

3) a) (5 pts) List five design and process parameters (not electrical or environmental) that effect the magnitude of I_{ds}.

b) (5 pts) Compute the gain factor (β) of the p-channel transistor given the following:

$\mu_p = 200\frac{\text{cm}^2}{\text{V-sec}}$

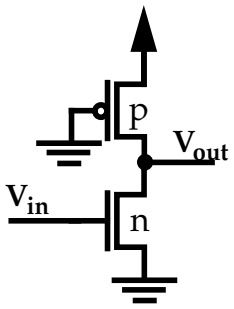
$\varepsilon = 3.9\varepsilon_0 = 3.9 \times 8.85 \times 10^{-14}\text{F/cm}$

$t_{ox} = 10\text{nm}$

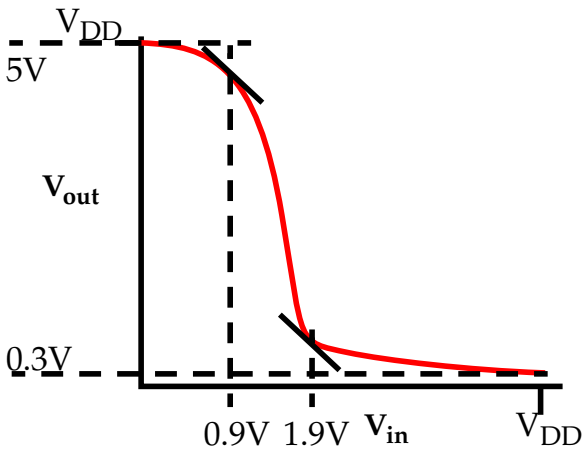
$\frac{W}{L} = 3$

c) (5 pts) What is the value of I_{ds} of this p-channel device given V_T = -0.5V, V_{GS}=-3.3V and V_{DS} = -2.0V. (Hint: First determine the region of operation).

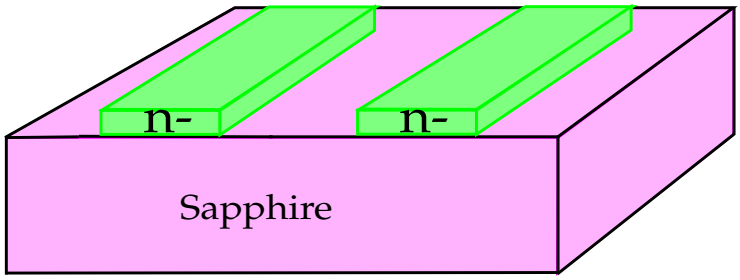
d) (5pts)Compute the noise margins (NM_H and NM_L) for the pseudo-nMOS inverter using the transfer curve.



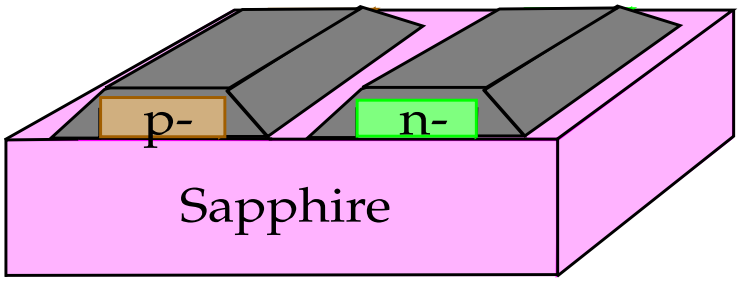
Pseudo-nMOS inverter



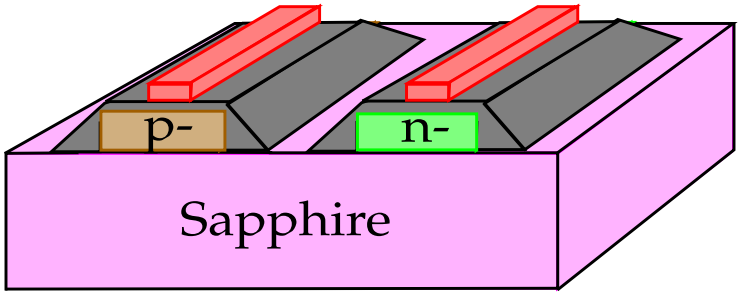
4) a) (8 pts) Give a one or two sentence description of the process step performed to produce each of the following transformations in the Silicon-On-Insulator process.



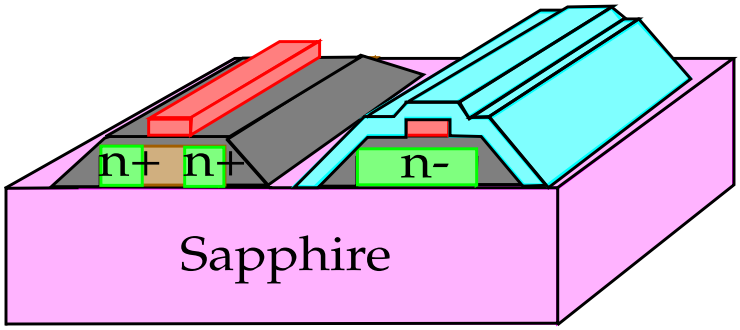
a)



b)



c)



d)

b) (6 pts) Give three (of five) advantages of Silicon-On-Insulator technology.

c) (6pts) Briefly describe the primary advantage of each of following CMOS process enhancements.

Additional levels of metal interconnect:

Reduction of polysilicon, source and drain diffusion sheet resistance using a refractory metal:

The use of local interconnect: