VHDL Keywords

abs	entity	next	select
access	exit	nor	severity
after	file	not	signal
alias	for	null	shared
all	function	of	sla
and	generate	on	sll
architecture	generic	open	sra
array	group	or	srl
assert	guarded	others	subtype
attribute	if	out	then
begin	impure	package	to
block	in	port	transport
body	inertial	postponed	type
buffer	inout	procedure	unaffected
bus	is	process	units
case	label	pure	until
component	library	range	use
configuration	linkage	record	variable
constant	literal	register	wait
disconnect	loop	reject	when
downto	map	rem	while
else	mod	report	with
elsif	nand	return	xnor
end	new	rol	xor