

Laboratory 6 worksheet

Name:

Section:

T.A:

Tutorial Section

Answer the following questions:

1. What process translates the HDL (hardware description language) into a netlist?
2. What does an accumulator do?
3. What is the difference between a CLB and an IOB?
4. Why is it good to be able to reuse sections of code for different projects?
5. An FPGA loses its programming when the power is removed. Think of a reason or application where this would be a good thing. Does a CPLD behave in the same way?
6. In Floorplanner, on a SpartanXL, what three things make up a CLB? How many CLB is using your design?
7. Draw a block diagram of the circuit implemented by the top.vhd file

Assignment Section

1. Draw a block diagram of the system you are asked to implement.
2. Demonstrate your system working to your T.A. and ask him/her to sign your worksheet.
3. How many CLBs is using your design?
4. Attach the top.vhd file of your design