

Lab 7- In depth Exploration of Floorplanner and XPower

Objectives:

1. Perform a more in depth analysis of device development using Floorplanner.
2. Perform an in-depth analysis of device development using XPower.

Assignment:

Create a new project and add the following code as a VHDL Module.

```

library IEEE;
use IEEE.std_logic_1164.all;

entity subtraction is
port (
BROW_IN: in STD_LOGIC;
XY_IN: in STD_LOGIC_VECTOR (1 downto 0);
BROW_OUT: out STD_LOGIC;
DIV_OUT: out STD_LOGIC
);
end subtraction;

architecture subtraction_arch of subtraction is
begin
-- 4 to 1 multiplexer design with case construct
-- SEL: in STD_LOGIC_VECTOR(1 downto 0);
-- A, B, C, D:in STD_LOGIC;
-- MUX_OUT: out STD_LOGIC;
OUT_DIV:
process (XY_IN, BROW_IN)
begin
case XY_IN is
when "00" => DIV_OUT <= BROW_IN;
when "01" => DIV_OUT <= not(BROW_IN);
when "10" => DIV_OUT <= not(BROW_IN);
when "11" => DIV_OUT <= BROW_IN;
when others => DIV_OUT <= 'Z';
end case;
end process;

-- 4 to 1 multiplexer design with case construct
-- SEL: in STD_LOGIC_VECTOR(1 downto 0);
-- A, B, C, D:in STD_LOGIC;
-- MUX_OUT: out STD_LOGIC;
OUT_BROW:
process (XY_IN, BROW_IN)
begin
case XY_IN is
when "00" => BROW_OUT <= BROW_IN;
when "01" => BROW_OUT <= '1';
when "10" => BROW_OUT <= '0';
when "11" => BROW_OUT <= BROW_IN;
when others => DIV_OUT <= 'Z';
end case;

```

```
end process;  
end subtraction_arch;
```

This is the binary subtractor from Lab 2. Use Floorplanner to place the design on the chip and XPower to analyze the power usage.

Deliverables

1. Your floorplanner view showing that the logic will fit into one CLB. You may assign your input and output to any IOBs you like.
2. Use XPower and show two different Total Power values by increasing and decreasing VCCInt.
3. By using XPower's Power Report, print out two reports showing the differences in Total Power when your inputs are set to 0 MHz and then again when they are set to 100 MHz.