

# **LABORATORY SESSION 5**

## **FINAL REPORT**

Name:

Section:

Date:

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## **Design Analysis**

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Draw a block diagram of what would be an 8-bit wide ripple carry adder.

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### **Creating, synthetizing and simulating a Half Adder (HA)**

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Step 1

Write down the instantiation code for the XOR and AND gate

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### **Creating, synthetizing and simulating a Full Adder (FA)**

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Step 2

Write down the instantiation code for the two half adders blocks and the OR gate.

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### **Creating, synthetizing and simulating a 4-bit Full Adder (FA)**

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Step 3

Write down the process for signals A, B and c\_in in your test bench.

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**Creating, synthesizing and simulating an Accumulator**

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Step 4

Write down the instantiation code for the adder and the register.

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**Implementing the Accumulator**

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Step 5

Demonstrate the system to the T.A

T.A signature:

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**Resources Analysis**

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Step 6

How many CLBs is using your system?

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**Final Task**

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Step 7

Demonstrate the system to the T.A

T.A signature:

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**Bonus Activity**

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Step 8

Demonstrate the system to the T.A

T.A signature:

1. How many CLBs is using your system? Is it more or less than the original design? Why?
2. Print down your code for the accumulator and attach it to your final report.