

Lab 3 Manual - Introduction to Arithmetic circuits

Introduction

In this lab you will design two subtractors using 4x1 and 8x1 Mux as seen in the lecture notes. You will be required to breadboard the design, implement it in VHDL and simulate it.

Goals

After completing this lab, you will be able to:

- Breadboard basic arithmetic circuits
- Use VHDL to implement basic arithmetic circuits

Breadboard the Circuit

Step 1

Design a full subtractor (inputs: A, B, Borrow in; outputs: Difference and Borrow out) circuit using 4-to-1 Multiplexers. Plan your work by completing **Part 1** of the worksheet. Use the logic trainer, breadboard the subtractor circuit and demonstrate it to your TA.

Start Project Navigator and Create the Project

Step 2

Almost all the code for this project is provided. As you did in Lab 2 create a new directory for your project with the following format: **C:/ece238/spring2005/student_name/lab3**. Add the files **Lab3_1.vhd** and **Lab3_1_tb.vhd** (these files are posted in the lab website) to your new directory.

You will need a bigger device in order to store this project. When you create your project in Xilinx use the settings in Figure 1.

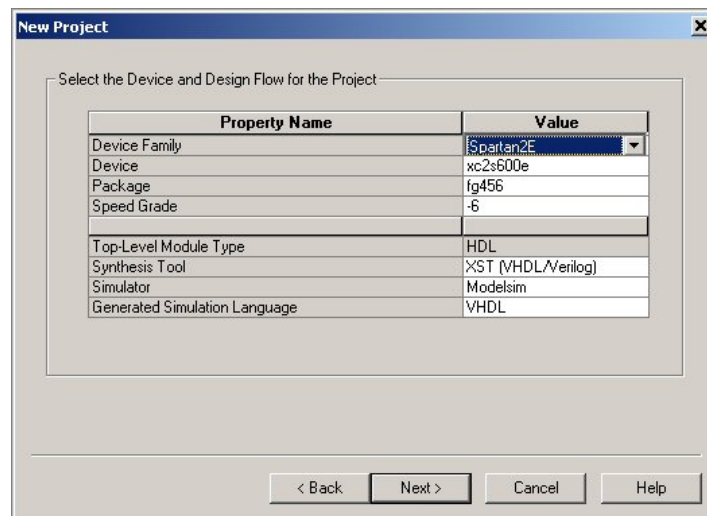


Figure 1: Project Settings

Analyze and Compile the Code

Step 3

Open the file Lab3_1.vhd. Read the code, analyze it and make sure you understand what the code is describing. Note that the code is incomplete, you will need to fill in the correct output for each set of inputs for BROW_OUT.

After completing the missing information in the code, compile **Lab3_1.vhd**. Make sure there are no errors or warnings.

Simulate the system

Step 4

The next step is to simulate this design. As you did in lab 2, simulate the design with ModelSim. Make sure the simulation waveform agrees with the truth table for the subtractor. In order to be sure the system is behaving in the right way, you need to simulate each and every input combination.

Final Task

Step 5

Repeat Steps 1-4 to design a subtractor using 8-to-1 multiplexers.