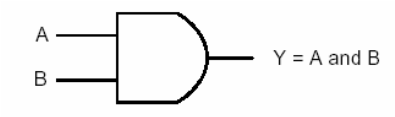
Lecture Notes – Lab 1

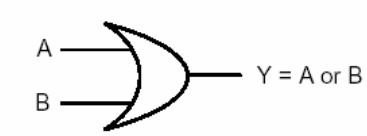
Basic logic gates

And Gate



A	B	Y=AB
0	0	0
0	1	0
1	0	0
1	1	1

Or Gate

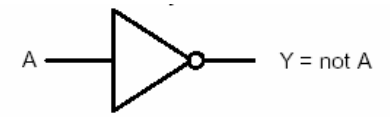


A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Lecture Notes – Lab 1

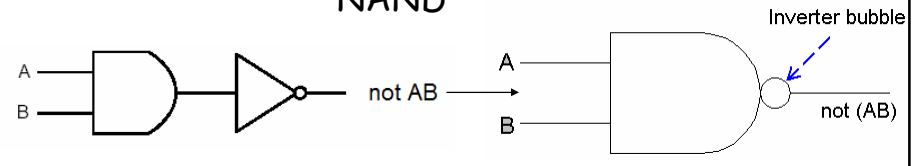
Basic logic gates

Inverter



A	Y=notA
0	1
1	0

NAND



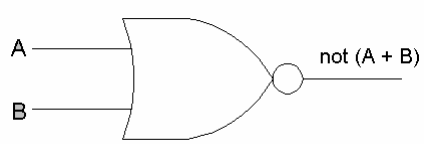
Elementary Theorem - Identity

X*1 = X; X*0 = 0 X + 1 = 1; X + 0 = X

Lecture Notes – Lab 1

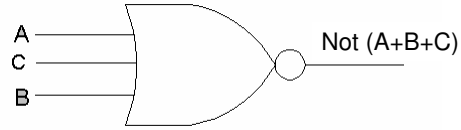
Logic gates

Nor Gate



A	B	A+B	Y=not(A+B)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Create two-input Nor with three-input Nor



We Want

Not (A+B+C) = Not (A+B)

C = ?

Lecture Notes – Lab 1

Example 1

Design a circuit for the following function:

F3= (Y + Z') X + X'YZ

X Y Z	X'	Z'	Y + Z'	(Y + Z') X	X'Y Z	F3
0 0 0	1	1	1	0	0	0
0 0 1	1	0	0	0	0	0
0 1 0	1	1	1	0	0	0
0 1 1	1	0	1	0	1	1
1 0 0	0	1	1	1	0	1
1 0 1	0	0	0	0	0	0
1 1 0	0	1	1	1	0	1
1 1 1	0	0	1	1	0	1

F3= XY + XZ' + X'YZ

F3 equals 1 when XY or XZ' or X'YZ equals 1

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K-maps

F3= (Y + Z') X + X'YZ

X Y Z	X'	Z'	Y + Z'	(Y + Z') X	X'Y Z	F3
0 0 0	1	1	1	0	0	0
0 0 1	1	0	0	0	0	0
0 1 0	1	1	1	0	0	0
0 1 1	1	0	1	0	1	1
1 0 0	0	1	1	1	0	1
1 0 1	0	0	0	0	0	0
1 1 0	0	1	1	1	0	1
1 1 1	0	0	1	1	0	1

1- Map TT to K-map

2- Simplify the boolean function

		Y Z			
		00	01	11	10
X	0	0	0	1	0
	1	1	0	1	1

		Y Z			
		00	01	11	10
X	0	0	0	1	0
	1	1	0	1	1

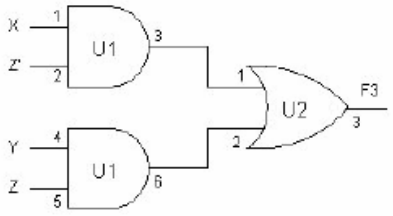
F3 = Y Z + XZ'

Lecture Notes – Lab 1

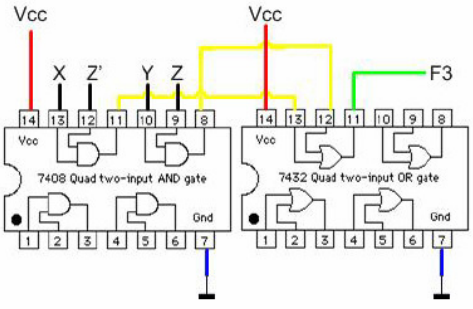
Design an AND/OR circuit

F3= YZ + XZ'

Logic diagram



Layout diagram - position on the breadboard



Lecture Notes – Lab 1

Example 2

Consider the following 4 variable function:

F4= B'CE'+ A'B'E'+ AC'E'+ ABC'E

A B C E	A'	B'	C'	E'	B'CE'	A'B'E'	AC'E'	ABC'E	F4
0 0 0 0	1	1	1	1	0	1	0	0	1
0 0 0 1	1	1	1	0	0	0	0	0	0
0 0 1 0	1	1	0	1	1	1	0	0	1
0 0 1 1	1	1	0	0	0	0	0	0	0
0 1 0 0	1	0	1	1	0	0	0	0	0
0 1 0 1	1	0	1	0	0	0	0	0	0
0 1 1 0	1	0	0	1	0	0	0	0	0
0 1 1 1	1	0	0	0	0	0	0	0	0
1 0 0 0	0	1	1	1	0	0	1	0	1
1 0 0 1	0	1	1	0	0	0	0	0	0
1 0 1 0	0	1	0	1	1	0	0	0	1
1 0 1 1	0	1	0	0	0	0	0	0	0
1 1 0 0	0	0	1	1	0	0	1	0	1
1 1 0 1	0	0	1	0	0	0	0	1	1
1 1 1 0	0	0	0	1	0	0	0	0	0
1 1 1 1	0	0	0	0	0	0	0	0	0

Lecture Notes – Lab 1

1- Maps the TT to K-map

		C E			
		00	01	11	10
A B	00	1	0	0	1
	01	0	0	0	0
	11	1	1	0	0
	10	1	0	0	1

2- Simplify the boolean function

		C E			
		00	01	11	10
A B	00	1	0	0	1
	01	0	0	0	0
	11	1	1	0	0
	10	1	0	0	1

F4 = B'E'+ ABC'

Lecture Notes – Lab 1

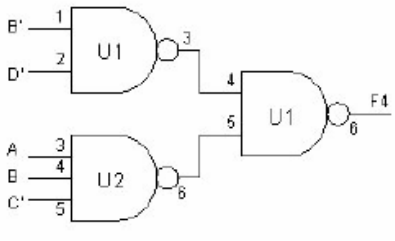
Design a NAND circuit: F4= B'E' + ABC'

F4 = F4'' = ((B'E' + ABC')')'

F4 = ((B'E')' (ABC')')'

By using Demorgan's identity

Logic diagram



Layout diagram