

Name \_\_\_\_\_  
Date \_\_\_\_\_  
Section \_\_\_\_\_

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## Lab 2 Worksheet

1. Draw the truth table for the equation  $Y = A'B + CD$
2. Describe the circuit using VHDL and simulate it. (Hint: Take the files and projects developed in the lab manual and modify it accordingly to the new equation.)
3. Simulate the new design and check it against the truth table from question 1.

Turn in a copy of your VHDL code file

Turn in a copy of the simulation waveform showing all possible combinations of inputs.