

ECE238

Lab Homework #2 (6 % Lab Grade)

Due Wednesday, July 5th at noon

Please do not send your homework via email; turn in a printed version of your work.

Problem 1.

Write 2 VHDL descriptions, sm1.vhd (Figure 1) and sm2.vhd (Figure 2), for the Moore state machines shown below. Both state machines accept as inputs X , $reset$ and clk , and have as output a bit $output$. Test the state machine 1 with the input sequence $X = "01001100110"$, and the state machine 2 with the input sequence $X = "0001000100110"$. Turn in sm1.vhd, sm2.vhd and the two waveforms for the above mentioned test cases.

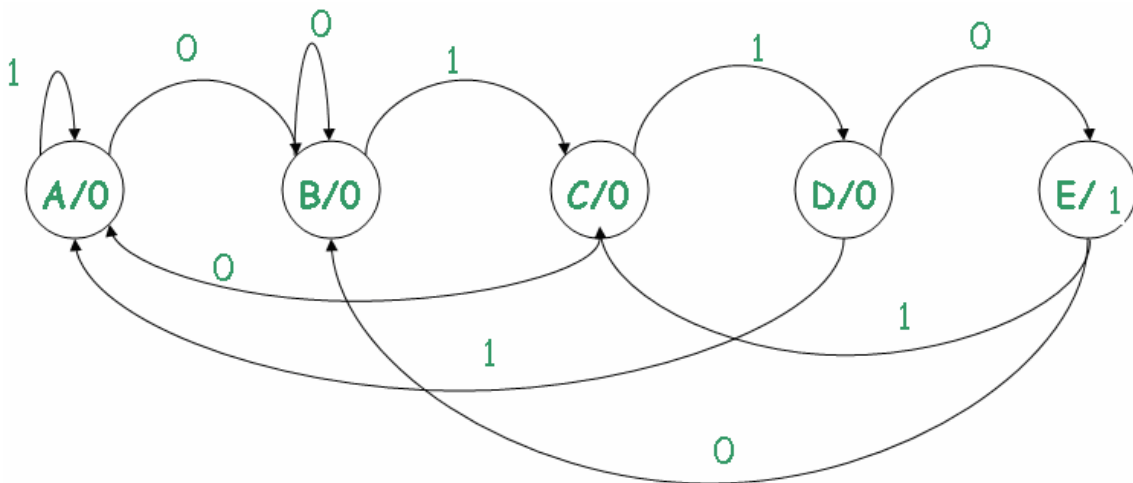


Figure 1. State machine 1.

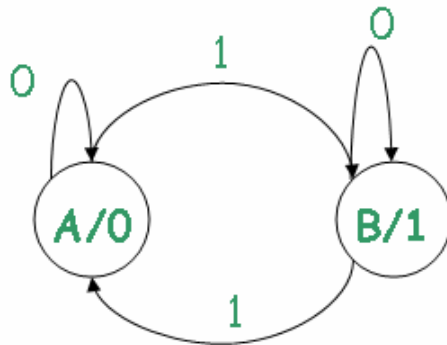


Figure 2. State machine 2.

Problem 2.

Write a VHDL description, `sys.vhd`, for the system showed in Figure 3. The system accepts the inputs `X`, `clk` and `reset`, and has as output a bit *output*. Test your system with the input `X = "010011001101100000110"`. Turn in `sys.vhd` and the waveform for the above mentioned test case.

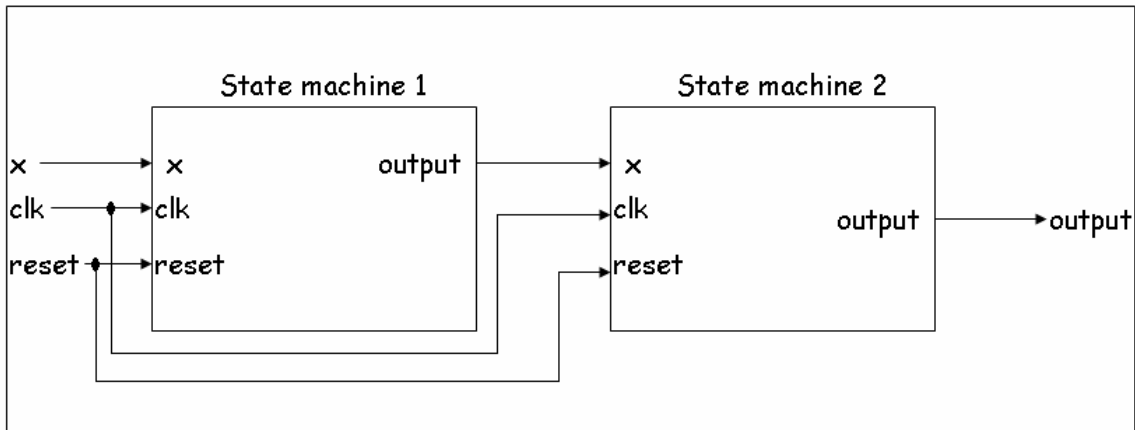


Figure 3.