

Name _____

Date _____

Section _____

1

Lab 6 Worksheet

Synthesize and Simulate the Counter

Step 2

- Draw the waveforms you will implement to test the counter. Attach the VHDL code of your testbench to the final report.

- Modify your testbench to have reset \leq '1' and pause \leq '1' together at the same time. What happens? Why? (Hint: Check the VHDL description of the counter to find out the answer).

Adding the Display Controller to the Project

Step 4

- What happens when you change the value of the potentiometer? Explain to your T.A. what's happening.

Project Testing

Step 7

- Demonstrate your system to the T.A. T.A. signature:

Final Task

Step 8

- Draw a block diagram of your system

- Demonstrate your system to the T.A.
- T.A. signature:

Bonus Activity

Step 9

- Demonstrate your system to the T.A. T.A. signature: